INTEGRATED CIRCUITS

DATA HANDBOOK

FAST TTL Logic Series
Supplement to IC 15

BOOK IC15 1991

Philips Components

PHILIPS

FAST TTL LOGIC SERIES

SUPPLEMENT

PREFACE

Since the publication of the 1990 FAST Logic Data Handbook, twenty-four new products have been released. Product specifications for these products are contained in this supplement and supercede any previously published "Preliminary Specifications".

74F189A	74F711	74F1763	74F8960
74F219A	74F712	74F1766	74F8962
74F646A	74F723	74F3893	74F8963
74F648A	74F725	74F5074	74F50109
74F651A	74F777	74F5300	74F50728
74F652A	74F807	74F5302	74F50729

A series of Industrial Temperature part types, guaranteed over an extended temperature range of -40°C to +85°C (instead of the traditional temperature range of 0°C to + 70°C) has also been released. Specifications for these parts and ordering information has been added to the existing data sheets. An "I" prefix has been added to designate the industrial temperature range part types:

I74F86	I74F244B	I74F656A	I74F3037
I74F112	I74F280B	I74F657	
I74F175	I74F655A	I74F776	

Development of the following part types listed as "preliminary" in the 1989 FAST Logic Data Handbook has been discontinued and these should not be considered as valid part types:

74F657A	74F1761	74F4763

Additional changes, corrections, or additions to existing specifications have been made and are included in this supplement for reference. Only those pages of individual product specifications which had a change, correction, pr addition are included along with the first page of the product specification. All revised areas have been highlighted by a bold dotted square to facilitate locating the change.

Four application notes AN219, AN222, AN220 and AN222 which support the 74F50XXX family are contained in this supplement. These application notes are not in the 1989 FAST Data Manual.

This booklet is a supplement to the 1990 FAST Logic Data Handbook and should be used in conjunction with it.

Product Status

FAST Logic Products

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Numerical index (supplement data sheets)

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Supplement data sheets

Document No.	853-1122
ECN No.	98618
Date of issue	November 27, 1989
Status	Product Specification
FAST Products	

FAST 74F06, 74F07 Inverter/Buffer/Drivers

74F06 Hex Inverter Buffer/Driver (Open Collector)
74F07 Hex Buffer/Driver (Open Collector)

FEATURES

- **Open Collector output drive 64mA**
- **High speed**
- **12V output termination voltage**
- **Symmetrical propagation delays**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F06	3.5ns	18mA
74F07	4.5ns	21mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F06N, N74F07N
14-Pin Plastic SO	N74F06D, N74F07D

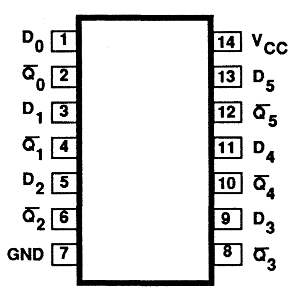
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data input	1.0/1.0	20μA/0.6mA
$\overline{Q}_n$	Data output ('F06)	OC/106.7	OC/64mA
Q_n	Data output ('F07)	OC/106.7	OC/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. OC = Open Collector.

PIN CONFIGURATION

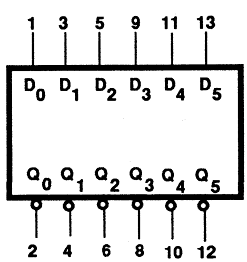
74F06



TOP VIEW

LOGIC SYMBOL

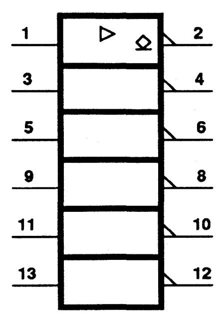
74F06



V_{CC} =pin 14
GND =pin 7

LOGIC SYMBOL(IEEE/IEC)

74F06



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS Min	LIMITS Nom	LIMITS Max	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			12	V
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{OH} =MAX, V_{IH} = MIN					250	µA
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX	±10%V_{CC}		0.30	0.50	V
						±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{CC}	Supply current [total]	74F06	I_{CCH}	V_{CC} = MAX				5.0	8.0	mA
			I_{CCL}					30	43	mA
		74F07	I_{CCH}					10	14	mA
			I_{CCL}					32	45	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 100Ω Min	Typ	Max	T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 100Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to $\bar{Q}_n$	74F06	Waveform 1	2.0 1.5	3.5 3.0	6.0 5.5	1.5 1.0	6.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F07	Waveform 2	2.0 3.0	4.0 5.0	6.0 7.0	2.0 2.5	6.5 7.5	ns

Document No.	853-0335
ECN No.	99598
Date of issue	May 15, 1990
Status	Product Specification
FAST Products	

FAST 74F74 FLIP-FLOP

Dual D-Type Flip-Flop

DESCRIPTION

The 74F74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock (CP) input.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are synchronously
active Low inputs and operate independently of the clock (CP). When Set and Reset are inactive (High), Data at the D input is transferred to the Q and $\overline{Q}$ outputs on the Low-to-High transition of the Clock. Data must be stable just one setup time prior to the Low-to-High transition of the clock for predictable operation.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F74	125 MHz	11.5mA

ORDERING INFORMATION

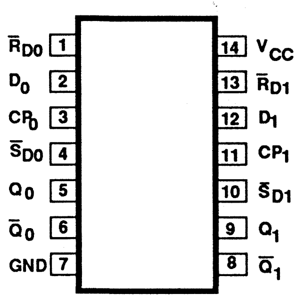
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F74N
14-Pin Plastic SO	N74F74D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/1.0	20µA/0.6mA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{S}_{D0}$, $\overline{S}_{DI}$	Set inputs (active Low)	1.0/3.0	20µA/1.8mA
$\overline{R}_{D0}$, $\overline{R}_{DI}$	Reset inputs (active Low)	1.0/3.0	20µA/1.8mA
Q_0, Q_I, $\overline{Q}_0$, $\overline{Q}_I$	Data outputs	50/33	1.0mA/20mA

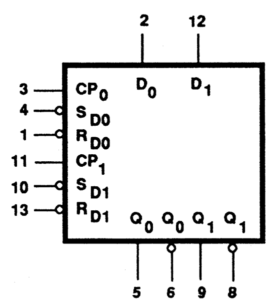
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



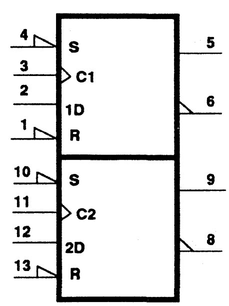
TOP VIEW

LOGIC SYMBOL

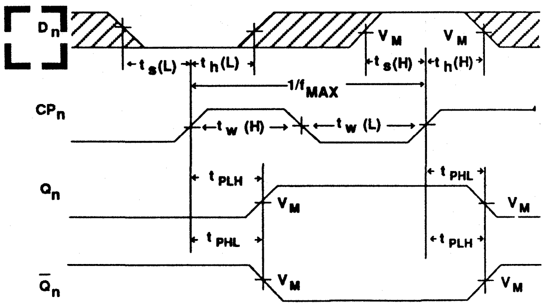


V_{CC} =pin 14
GND =pin 7

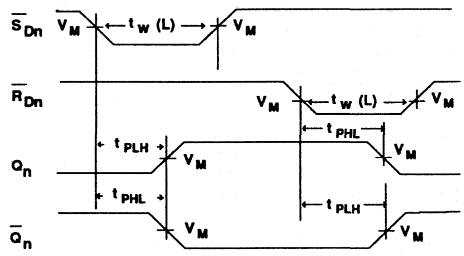
LOGIC SYMBOL(IEEE/IEC)



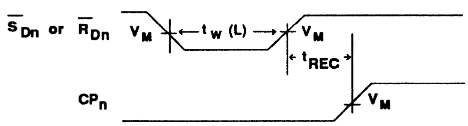
AC WAVEFORMS



Waveform 1. Propagation Delay For data to output, data setup time and hold times, clock width, and maximum clock frequency



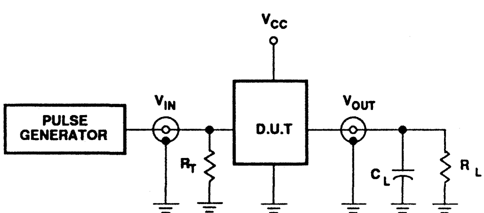
Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width



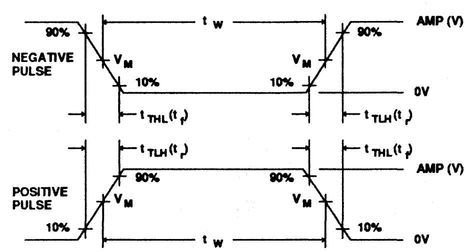
Waveform 3.
Reset pulse width, and recovery time for reset to clock

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0055
ECN No.	99494
Date of issue	April 27, 1990
Status	Product Specification
FAST Products	

FAST 74F85
Comparator

4-Bit Magnitude Comparator

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F85	7.0ns	40mA

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Magnitude comparison of any binary words**
- **Serial of parallel expansion without extra gating**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F85N
16-Pin Plastic SOL	N74F85D

DESCRIPTION

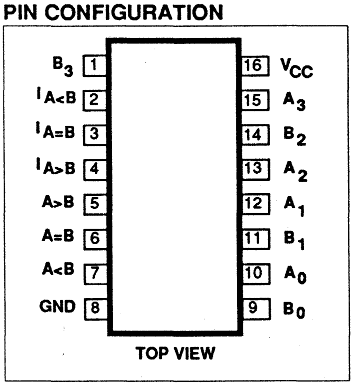
The 74F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A_0-A_3) and (B_0-B_3) where A_3 and B_3 are the most significant bits. The operation of the 74F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exists in the parallel expansion scheme. The expansion inputs $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A>B, A=B and A<B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ =Low, $I_{A=B}$=High and $I_{A<B}$=Low.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

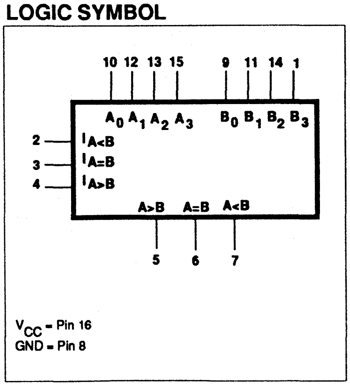
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_3	Comparing inputs	1.0/0.033	20μA/20μA
B_0- B_3	Comparing inputs	1.0/0.033	20μA/20μA
$I_{A<B}$, $I_{A=B}$, $I_{A>B}$	Expansion inputs (active High)	1.0/0.033	20μA/20μA
A<B, A=B, A>B	Data outputs (active High)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

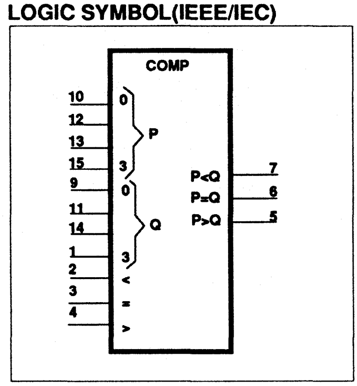
PIN CONFIGURATION



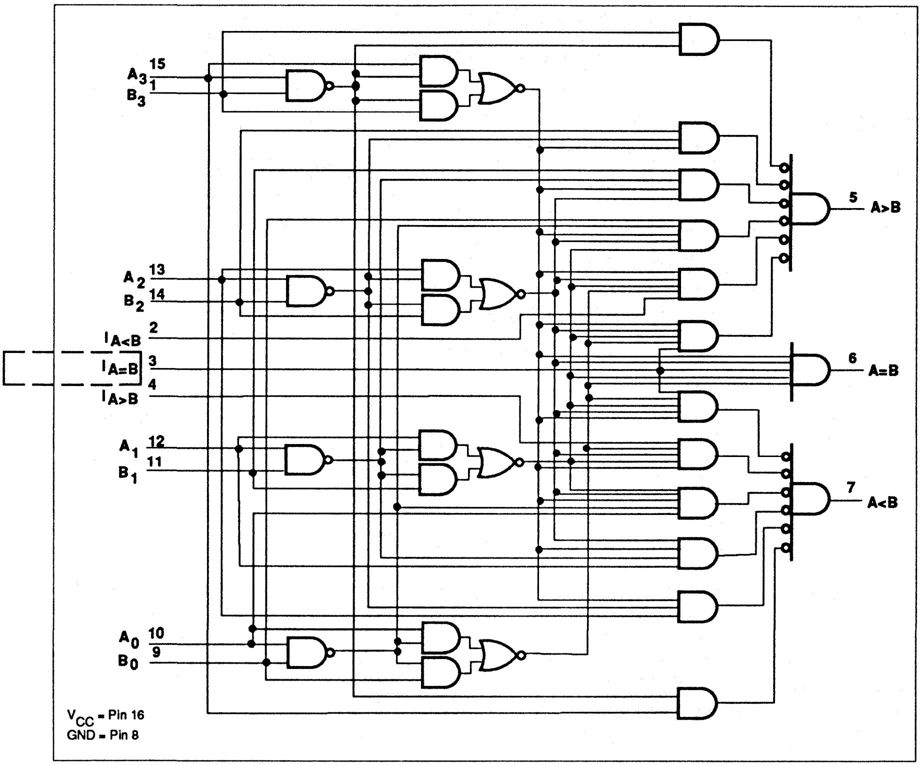
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

Document No.	853-0336
ECN No.	98773
Date of issue	February 9, 1990
Status	Product Specification
FAST Products	

FAST 74F86
Gate
Quad 2-Input Exclusive-OR Gate

FEATURE

- **Industrial temperature range available (-40°C to +85°C)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F86	4.3 ns	16.5 mA

FUNCTION TABLE

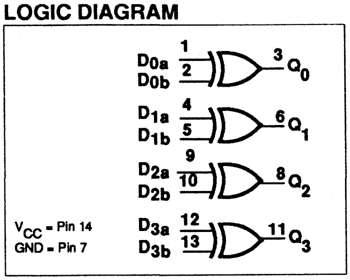
INPUTS		OUTPUT
D_{na}	D_{nb}	Q_n
L	L	L
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
14-Pin Plastic DIP	N74F86N	I74F86N
14-Pin Plastic SO	N74F86D	I74F86D

LOGIC DIAGRAM

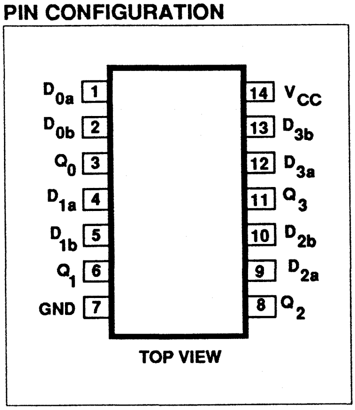


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

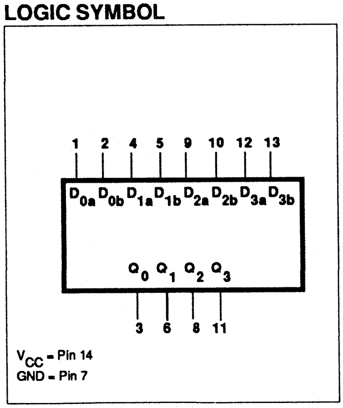
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20μA/0.6mA
Q_n	Data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

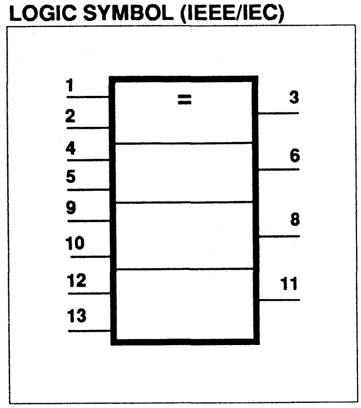
PIN CONFIGURATION



LOGIC SYMBOL



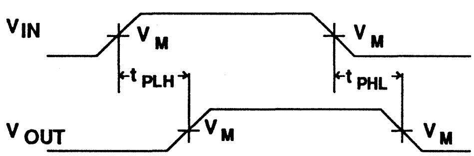
LOGIC SYMBOL (IEEE/IEC)



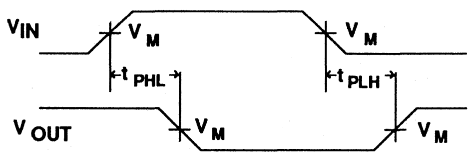
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		T_A = -40°C to +85°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na} or D_{nb} to Q_n (Other input Low)	Waveform 1	3.0 3.0	4.0 4.2	5.5 5.5	3.0 3.0	6.5 6.5	3.0 2.5	7.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay D_{na} or D_{nb} to Q_n (Other input High)	Waveform 2	3.5 3.0	5.3 4.7	7.0 6.5	3.5 3.0	8.0 7.5	3.5 3.0	10.0 8.0	ns

AC WAVEFORMS



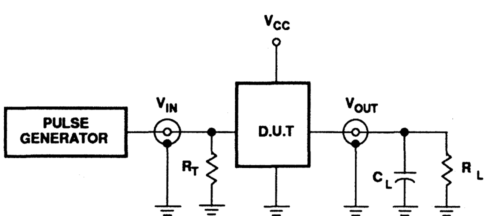
Waveform 1.
For Non-Inverting Outputs



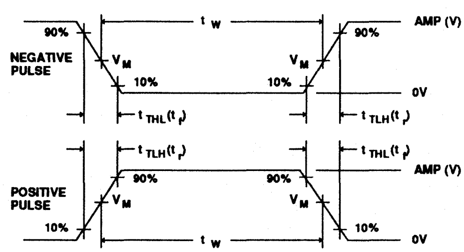
Waveform 2
For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0338
ECN No.	98775
Date of issue	February 9, 1990
Status	Product Specification
FAST Products	

FAST 74F112
Flip-Flop

Dual J-K Negative Edge-triggered Flip-Flop

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F112	100MHz	15mA

FEATURE

- **Industrial temperature range available (-40°C to +85°C)**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
16-Pin Plastic DIP	N74F112N	I74F112N
16-Pin Plastic SO	N74F112D	I74F112D

DESCRIPTION

The 74F112, Dual Negative Edge-Triggered JK-Type Flip-Flop, features individual J, K, Clock ($\overline{CP}_n$), Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, true (Q_n) and complementary ($\overline{Q}_n$) outputs.

The $\overline{S}_D$ and $\overline{R}_D$ inputs, when Low, set or reset the outputs as shown in the Function Table regardless of the level at the other inputs.

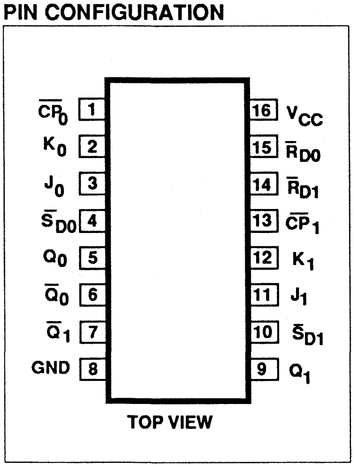
A High level on the clock ($\overline{CP}_n$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}_n$ is High and flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the $\overline{CP}_n$.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

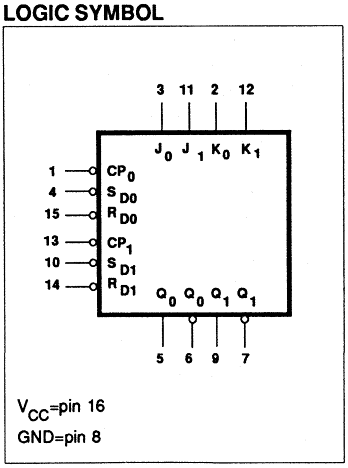
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/1.0	20µA/0.6mA
K_0, K_1	K inputs	1.0/1.0	20µA/0.6mA
$\overline{S}_{D0}, \overline{S}_{D1}$	Set inputs (active Low)	1.0/5.0	20µA/3.0mA
$\overline{R}_{D0}, \overline{R}_{D1}$	Reset inputs (active Low)	1.0/5.0	20µA/3.0mA
$\overline{CP}_0, \overline{CP}_1$	Clock Pulse input (active falling edge)	1.0/4.0	20µA/2.4mA
$Q_0, \overline{Q}_0$; $Q_1, \overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

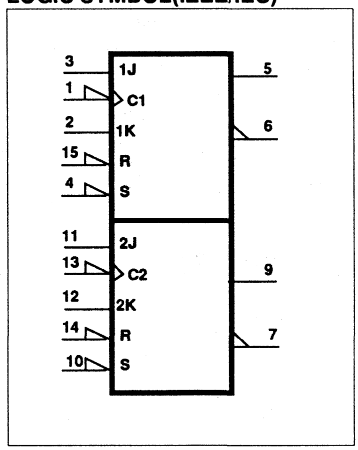
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



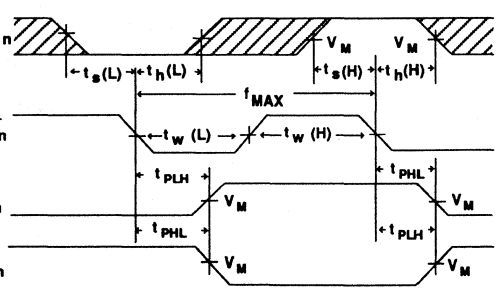
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		$T_A = -40°C$ to $+85°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	85	100		80		80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	5.0 5.0	6.5 6.5	2.0 2.0	7.5 7.5	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_D$ to Q_n or $\overline{Q}_n$	Waveform 2,3	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	1.5 1.5	7.5 7.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		$T_A = -40°C$ to $+85°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n, K_n to $\overline{CP}$	Waveform 1	4.0 3.5			5.0 4.0		5.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n, K_n to $\overline{CP}$	Waveform 1	0.0 0.0			0.0 0.0		0.0 0.0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse width High or Low	Waveform 1	4.5 4.5			5.0 5.0		5.0 5.0		ns
$t_w(L)$	$\overline{S}_{Dn}$, $\overline{R}_D$ Pulse width Low	Waveform 2,3	4.5			5.0		5.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$, $\overline{R}_D$ to $\overline{CP}$	Waveform 2,3	4.5			5.0		5.0		ns

AC WAVEFORMS



Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock pulse width

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Document No.	853-0342
ECN No.	98710
Date of issue	November 27, 1990
Status	Product Specification
FAST Products	

FAST 74F132
Schmitt Trigger
Quad 2-Input NAND Schmitt Trigger

DESCRIPTION

The 74F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates. Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mv) is determined by reisistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{T+MAX}, the gate will respond in the transition of the other input as shown in Waveform 1.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F132	6.3 ns	13 mA

ORDERING INFORMATION

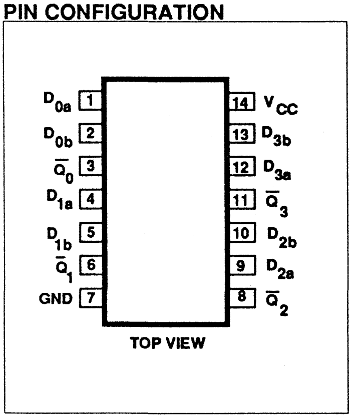
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F132N
14-Pin Plastic SO	N74F132D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

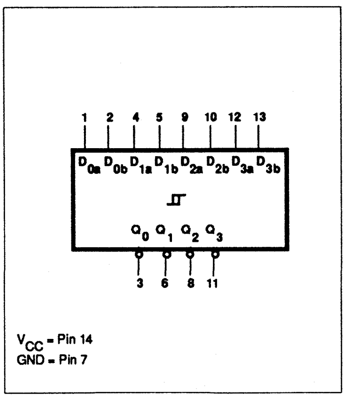
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_n$	Data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

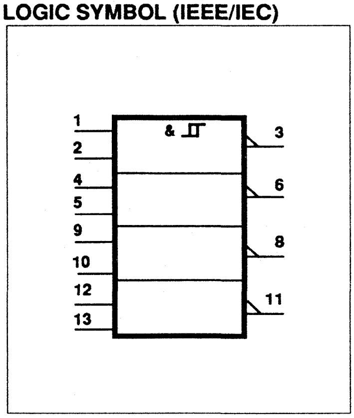
PIN CONFIGURATION



LOGIC SYMBOL



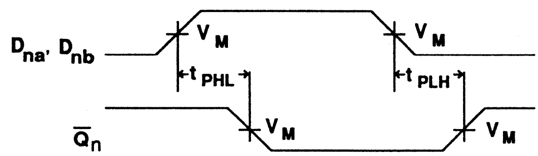
LOGIC SYMBOL (IEEE/IEC)



AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	3.5 4.5	5.5 6.0	7.0 8.0	3.0 4.5	8.5 8.5	ns

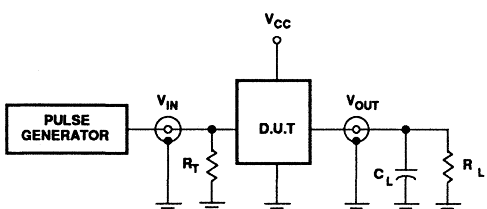
AC WAVEFORMS



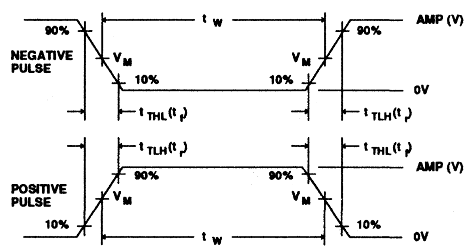
Waveform 1.
For Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

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ECN No.	97893
Date of issue	October 16, 1989
Status	Product Specification
FAST Products	

FAST 74F133
Gate

13-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F133	4.0 ns	2.0 mA

ORDERING INFORMATION

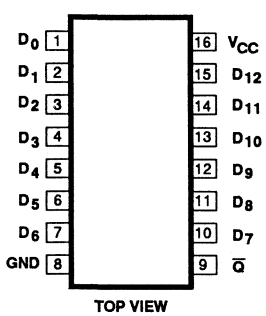
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F133N
14-Pin Plastic SO	N74F133D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

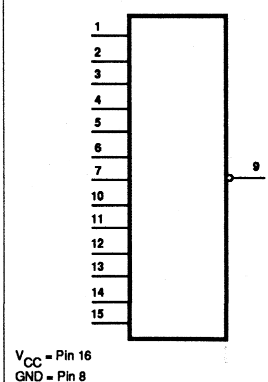
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0-D_{12}	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}$	Data Output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

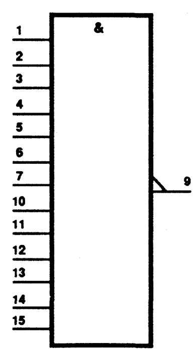
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Document No.	853-0344
ECN No.	98903
Date of issue	February 23, 1990
Status	Product Specification
FAST Products	

FAST 74F139

Decoder/Demultiplexer

Dual 1-of-4 Decoder//Demultiplexer

FEATURES

- **Demultiplexing capability**
- **Two independent 1-of-4 decoders**
- **Multifunction capability**

DESCRIPTION

The 74F139 is a high speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_{0n}, A_{1n}) and providing four mutually exclusive active-Low outputs ($\overline{Q}_{0n}$ - $\overline{Q}_{3n}$). Each decoder has an active-Low Enable ($\overline{E}$). When $\overline{E}$ is High, every output is forced High. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F139	5.3ns	13mA

ORDERING INFORMATION

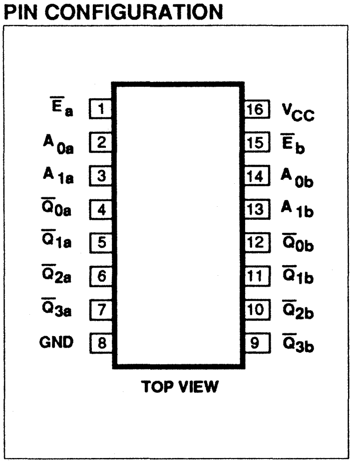
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F139N
16-Pin Plastic SO	N74F139D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

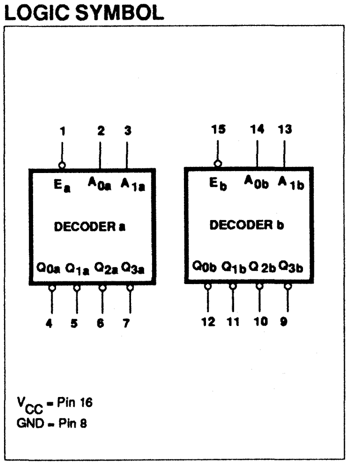
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_{na}, A_{nb}	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_a$, $\overline{E}_b$	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Q}_{0n}$ - $\overline{Q}_{3n}$	Data outputs (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

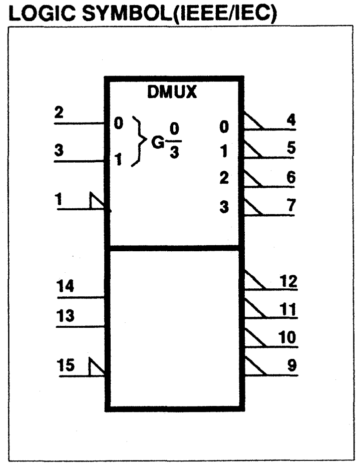
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Document No.	853-1155
ECN No.	98493
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F154
Decoder/Demultiplexer

1-of-16 Decoder/Demultiplexer

FEATURES

- **16-line demultiplexing capability**
- **Mutually exclusive outputs**
- **2-input enable gate for strobing or expansion**

DESCRIPTION

The 74F154 decoder accepts four active High binary address inputs and provides 16 mutually exclusive active Low outputs. The 2-input Enable ($\overline{E}_0$, $\overline{E}_1$) gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The Enable gate has two AND'ed inputs which must be Low to enable the outputs.

The 74F154 can be used as a 1-of-16 demultiplexer by using one of the Enable inputs as the multiplexed data input. When the other Enable is Low, the addressed output will follow the state of the applied data.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F154	5.5 ns	26mA

ORDERING INFORMATION

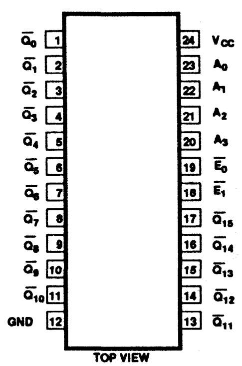
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F154N
24-Pin Plastic SOL	N74F154D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

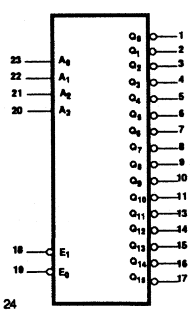
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Enable inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_0$ - $\overline{Q}_{15}$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

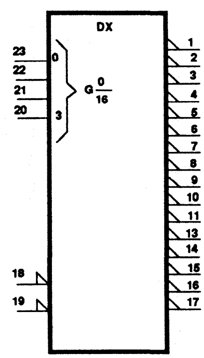


LOGIC SYMBOL

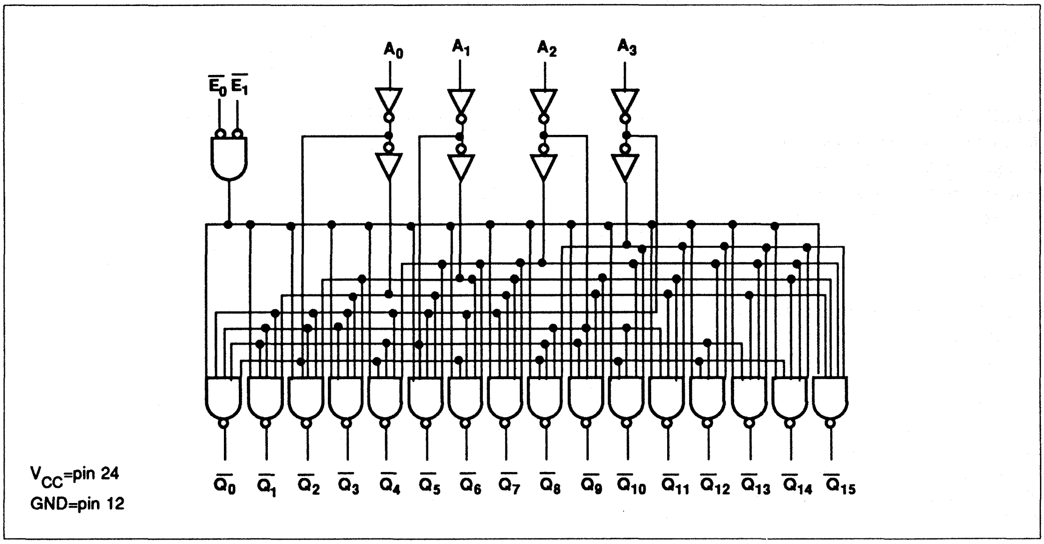


V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS															
$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$	$\overline{Q}_8$	$\overline{Q}_9$	$\overline{Q}_{10}$	$\overline{Q}_{11}$	$\overline{Q}_{12}$	$\overline{Q}_{13}$	$\overline{Q}_{14}$	$\overline{Q}_{15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

Document No.	853-0348
ECN No.	98770
Date of issue	February 8, 1990
Status	Product Specification
FAST Products	

FAST 74F164
Shift Register

8-Bit Serial-In Parallel-Out Shift Register

FEATURES
- **Gated serial data inputs**
- **Typical shift frequency of 100MHz**
- **Asynchronous Master Reset**
- **Fully buffered clock and data inputs**
- **Fully synchronous data transfers**

DESCRIPTION

The 74F164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered through one of two inputs (D_{sa}, D_{sb}); either input can be used as an active High enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input, and enters into Q_0 the logical AND of the the two data inputs (D_{sa}, D_{sb}) that existed one setup time before the rising clock edge. A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F164	100MHz	33mA

ORDERING INFORMATION

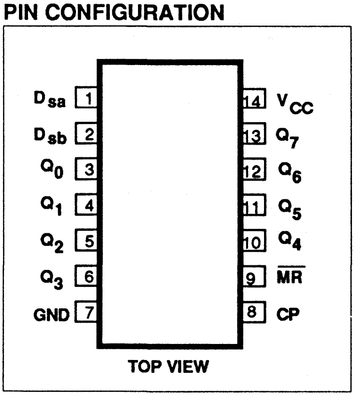
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F164N
14-Pin Plastic SO	N74F164D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

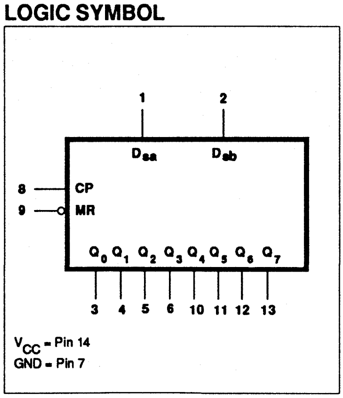
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{sa}, D_{sb}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

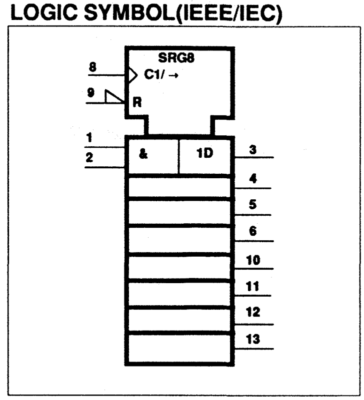
PIN CONFIGURATION



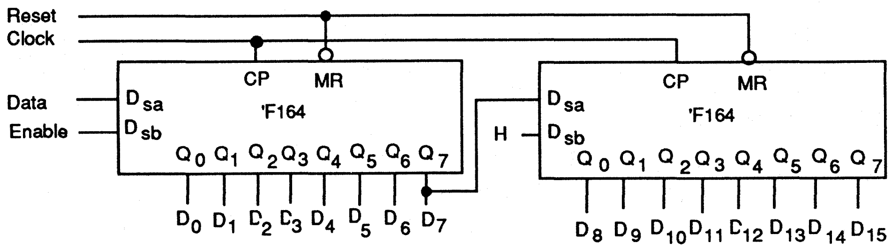
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



APPLICATION



NOTE: The 'F164 can be cascaded to form synchronous shift registers of longer length. Here, two 'F164 are combined to form a 16 bit shift register.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 5.0	5.0 7.0	8.0 10.0	2.5 5.0	9.0 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	5.5	7.5	10.5	5.5	11.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	7.0 7.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	1.0 1.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width High or Low	Waveform 1	4.0 7.0			4.0 7.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 2	7.0			7.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			7.0		ns

Document No.	853-0047
ECN No.	98776
Date of issue	February 9, 1990
Status	Product Specification
FAST Products	

FAST 74F175
Flip-Flop

Quad D Flip-Flop

FEATURES

- **Four edge-triggered D-type flip-flops**
- **Buffered common clock**
- **Buffered asynchronous Master Reset**
- **True and complementary outputs**
- **Industrial temperature range available (-40°C to +85°C)**

DESCRIPTION

The 74F175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously. The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output. All Q outputs will be forced Low independently of clock or data inputs by Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complementary outputs are required and the CP and $\overline{MR}$ are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F175	140MHz	25mA

ORDERING INFORMATION

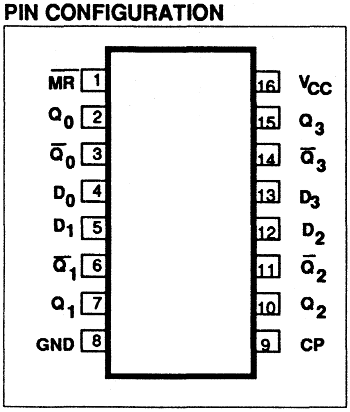
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
16-Pin Plastic DIP	N74F175N	I74F175N
16-Pin Plastic SO	N74F175D	I74F175D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

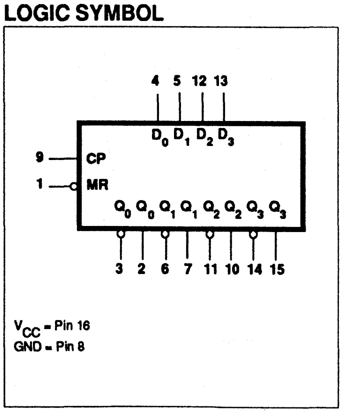
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
Q_0 - Q_3	True outputs	50/33	1.0mA/20mA
$\overline{Q}_0$ - $\overline{Q}_3$	Complementary outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

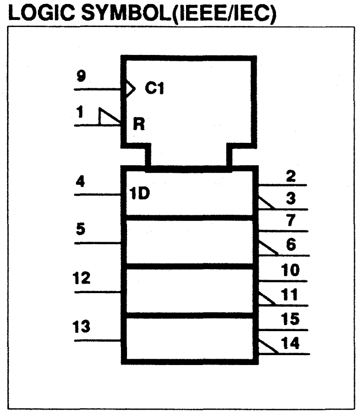
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		$T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	140		100		100		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n or $\overline{Q}_n$	Waveform 1	4.0 4.0	5.0 6.5	6.5 8.5	4.0 4.0	7.5 9.5	3.5 4.0	8.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	4.5	9.0	11.5	4.5	13.0	4.5	13.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}_n$	Waveform 3	4.0	6.5	8.0	4.0	9.0	4.0	11.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		$T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	3.0 3.0			3.0 3.0		3.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width High or Low	Waveform 1	4.0 5.0			4.0 5.0		4.0 6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 3	5.0			5.0		5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			5.0		6.0		ns

Document No.	853-1309
ECN No.	98908
Date of issue	February 23, 1990
Status	Product Specification
FAST Products	

FAST 74F189A

64-Bit TTL Bipolar RAM, Inverting (3-State)

FEATURES

- **High speed performance**
- **Replaces 74F189**
- **Address access time: 8 ns max vs 28ns for 74F189**
- **Power dissipation: 4.3 mW/bit typ**
- **Schottky clamped TTL**
- **One chip enable**
- **Inverting outputs (For non-inverting outputs see 74F219A)**
- **Buffered PNP inputs**
- **3-state outputs**
- **74F189A in 150 mil wide S.O. is preferred option for new designs**
- **C3F189A in 300 mil wide S.O.L. replaces 74F189 in existing designs**

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F189A	5ns	55mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F189AN
16-Pin Plastic SO (150 mil)	N74F189AD
16-Pin Plastic SOL (300 mil)	C3F189AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
A_0 - A_3	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Chip Enable input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{WE}$	Write Enable input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{Q}_0$ - $\overline{Q}_3$	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

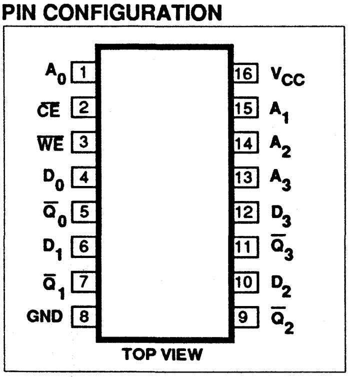
APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

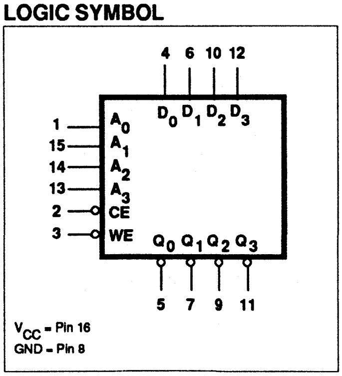
DESCRIPTION

The 74F189A is a high speed, 64-Bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are in High impedance state whenever the Chip Enable ($\overline{CE}$) is High. The outputs are active only in the READ mode ($\overline{WE}$ = High) and the output data is the complement of the stored data.

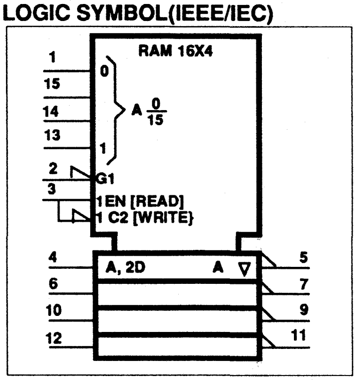
PIN CONFIGURATION



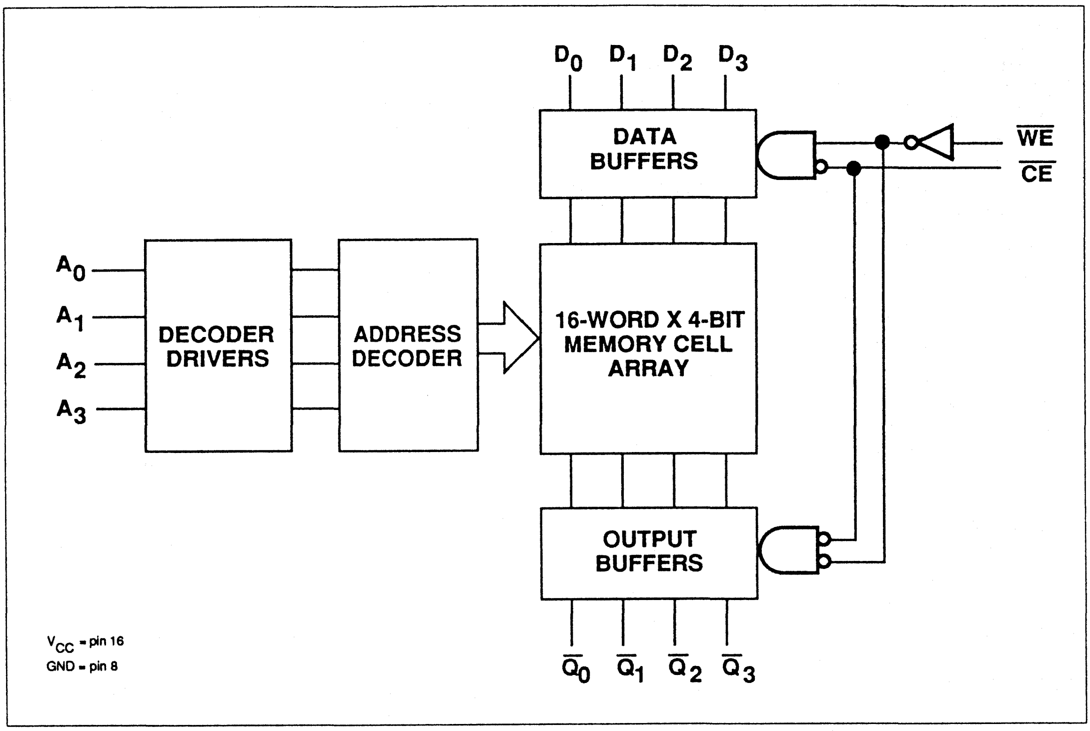
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
$\overline{CE}$	$\overline{WE}$	D_n	$\overline{Q}_n$	
L	H	X	Complement of stored data	Read
L	L	L	High impedance	Write "0"
L	L	H	High impedance	Write "1"
H	X	X	High impedance	Disable Input

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CE}$, $\overline{WE}$					-1.2	mA
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	mA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V				-50	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, $\overline{CE}$ = $\overline{WE}$ = GND			55	80	mA
C_{IN}	Input capacitance		V_{CC} = 5V, V_{IN} = 2.0V			4		pF
C_{OUT}	Output capacitance		V_{CC} = 5V, V_{OUT} = 2.0V			7		pF

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

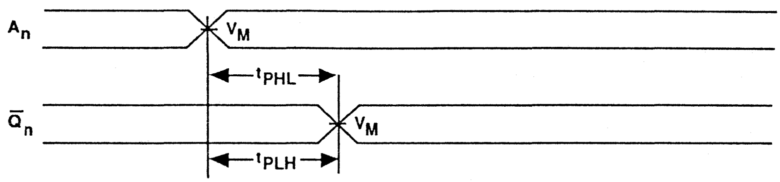
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Access time	Propagation delay A_n to $\overline{Q}_n$	Waveform 1	2.5 2.0	5.0 4.5	8.0 8.0	2.5 2.0	8.0 8.0	ns
t_{PZH} t_{PZL}	Access time	Enable time $\overline{CE}$ to $\overline{Q}_n$	Waveform 2	2.0 2.0	3.5 4.0	6.0 7.0	1.5 2.0	7.0 7.5	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{CE}$ to $\overline{Q}_n$		Waveform 3	2.5 1.5	4.5 3.0	7.0 5.5	2.0 1.5	8.0 6.0	ns
t_{PZH} t_{PZL}	Write Recovery time	Enable time $\overline{WE}$ to $\overline{Q}_n$	Waveform 4	2.0 2.5	4.0 4.5	6.5 7.5	2.0 2.5	7.0 8.0	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{WE}$ to $\overline{Q}_n$		Waveform 4	3.5 1.5	5.5 3.5	8.5 6.5	3.0 1.5	9.0 7.0	ns

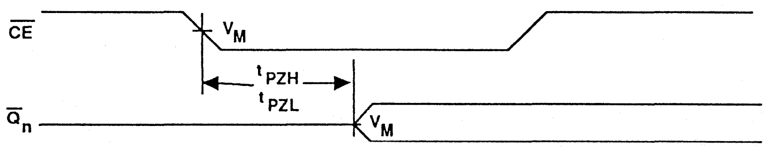
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time A_n to $\overline{WE}$	Waveform 4	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time A_n to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time D_n to $\overline{WE}$	Waveform 4	7.5 6.5			9.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_s(L)$	Setup time $\overline{CE}$ (falling edge) to $\overline{WE}$ (falling edge)	Waveform 4	0			0		ns
$t_h(L)$	Hold time $\overline{WE}$ (falling edge) to $\overline{CE}$ (rising edge)	Waveform 4	6.5			7.5		ns
$t_w(L)$	Pulse width, Low $\overline{WE}$	Waveform 4	7.0			8.0		ns

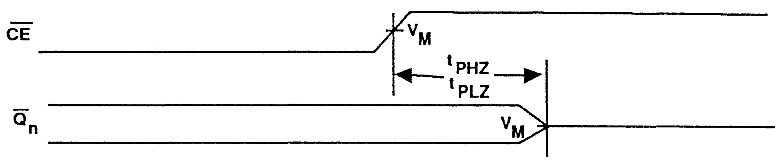
AC WAVEFORMS



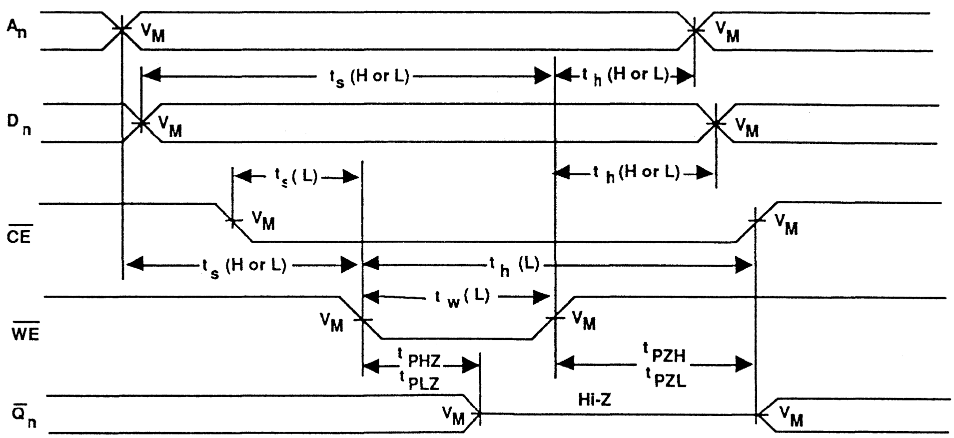
Waveform1. Read Cycle, Address Access Time



Waveform 2. Read Cycle, Chip Enable Access Time



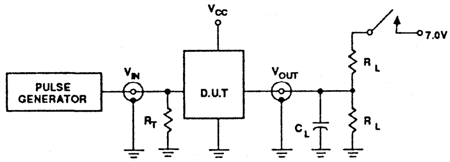
Waveform 3. Read Cycle, Chip Disable Time



Waveform 4. Write Cycle

NOTES: 1. For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

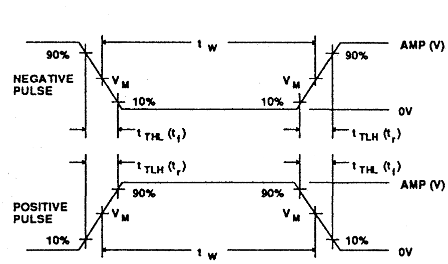
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0353
ECN No.	98486
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F192, 74F193 Counters

'F192 Up/Down Decade Counter With Separate Up/Down Clocks
'F193 Up/Down Binary Counter With Separate Up/Down Clocks

FEATURES

- **Synchronous, reversible 4-bit counting**
- **Asynchronous parallel load capability**
- **Asynchronous reset (clear)**
- **Cascadable without external logic**

DESCRIPTION

The 74F192 and 74F193 are 4-bit synchronous Up/Down Counters. The 74F192 counts in BCD mode and 74F193 counts in the binary mode. Separate up/down clocks, CP_U and CP_D, respectively simplify operation. The outputs change state synchronously with the Low-to-High transition of either clock input. If the CP_U clock is pulsed while CP_D is held High, the device will count up. If the CP_D clock is pulsed while CP_U is held High, the device will count down The device can be cleared at any time by the asynchronous reset pin. It may also be loaded in parallel by activating the asynchronous parallel load pin. Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, asynchronous preset, load, and synchronous count up and count down functions. Each flip-flop contains JK feedback from slave to master such that a Low-to-High transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one. One clock should be held High while counting with the other, because the circuit will either count by twos or not at all depending on the state of the first JK flip-flop, which cannot toggle as long as either clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.The terminal count up ($\overline{TC}_U$) and terminal count down ($\overline{TC}_D$) outputs are normally High. When the circuit has reached the maximum count state (9 for the 'F192 and 15 for the 'F193), the next High-to-Low transition of CP_U will cause $\overline{TC}_U$ to go Low. $\overline{TC}_U$ will stay Low until CP_U goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go Low when the circuit is in the zero state and CP_D goes Low. The $\overline{TC}$ outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous since there is a two-gate delay time difference added for each stage that is added. The counter may be preset by the asynchronmous parallel load capability of the circuit. Information present on the parallel data inputs D_0-D_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs when the Parallel Load ($\overline{PL}$) input is Low. A High level on the Master Reset (MR) input will disable the parallel load gates, override both clock inputs, and sets all Q outputs Low. If one of the clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of the clock will be interpreted as legitimate signal and will be counted.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F192	125MHz	32mA
74F193	125MHz	32mA

ORDERING INFORMATION

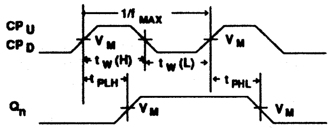
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	N74F192N, N74F193N
16-Pin Plastic SO	N74F192D, N74F193D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

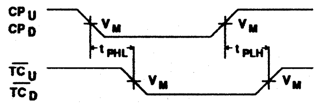
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
CP_U	Count up clock input (active rising edge)	1.0/3.0	20µA/1.8mA
CP_D	Count down clock input (active rising edge)	1.0/3.0	20µA/1.8mA
$\overline{PL}$	Asynchronous parallel load control input (active Low)	1.0/1.0	20µA/0.6mA
MR	Asynchronous Master Reset input	1.0/1.0	20µA/0.6mA
Q_0 -Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}_U$	Terminal count up (carry) output (active Low)	50/33	1.0mA/20mA
$\overline{TC}_D$	Terminal count down (borrow) output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

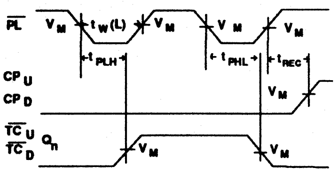
AC WAVEFORMS



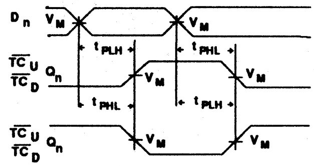
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



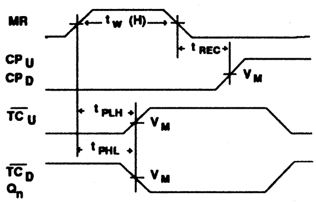
Waveform 2.
Propagation Delay, Clock to Terminal Count



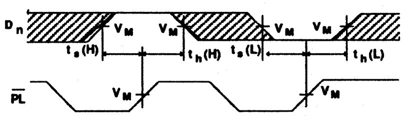
Waveform 3.
Parallel poulse width, Parallel Load to Output Delays, and Parallel Load to Clock Recovery Time



Waveform 4.
Propagation delay, Data to Flip-flop outputs, Terminal Count and Down Outputs



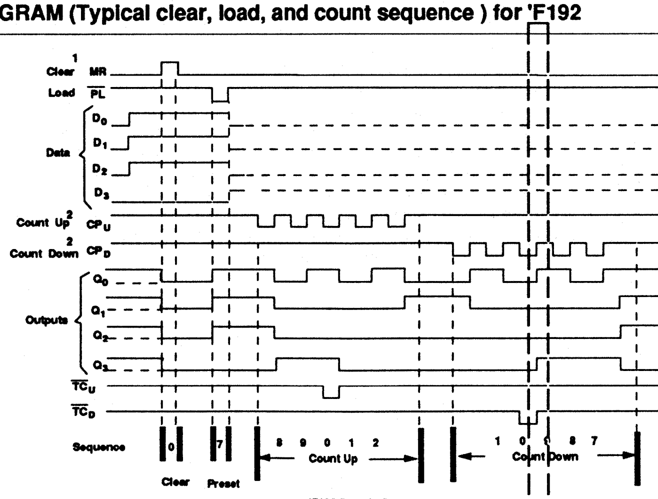
Waveform 5.
Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 6.
Data Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TIMING DIAGRAM (Typical clear, load, and count sequence) for 'F192



a. 'F192 Decade Counter

NOTES: 1. Clear overrides load data and count inputs.
2. When counting up, count down input must be High; when counting down, count up must be High.

Document No.	853-0024
ECN No.	97805
Date of issue	October 5, 1989
Status	Product Specification
FAST Products	

FAST 74F195
Shift Register

4-Bit Parallel-Access Shift Register

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F195	115MHz	45mA

FEATURES

- High-impedance NPN base inputs for reduced loading (20µA in Low and High states)
- Shift right and parallel load capability
- J - $\overline{K}$(D) inputs to first stage
- Complement output from last stage
- Asynchronous Master Reset

DESCRIPTION

The 74F195 is a 4-bit Parallel Access Shift Register and its functional characteristics are indicated in the Logic diagram and Function Table. The device is useful in a variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 74F195 operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$

ORDERING INFORMATION

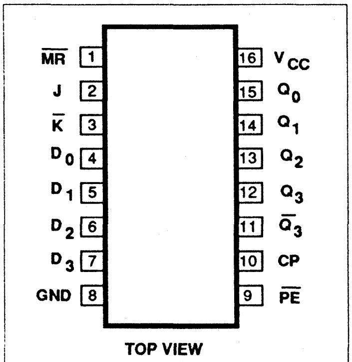
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V\pm10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F195N
16-Pin Plastic SO	N74F195D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

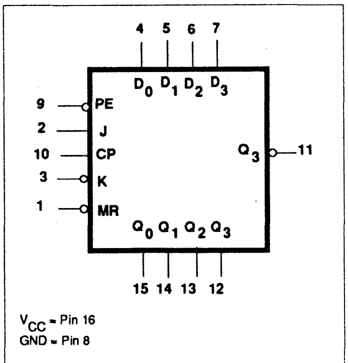
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Parallel data inputs	1.0/0.033	20µA/20µA
J, $\overline{K}$	J - K or D type serial inputs	1.0/0.033	20µA/20µA
$\overline{PE}$	Parallel Enable input	1.0/0.033	20µA/20µA
CP	Clock Pulse input (Active rising edge)	1.0/0.033	20µA/20µA
$\overline{MR}$	Master Reset input (Active Low)	2.0/0.066	40µA/40µA
Q_0 - Q_3, $\overline{Q}_3$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

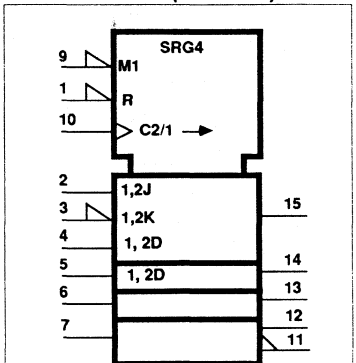
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Typ	Max	LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Max	UNIT
f_{MAX}	Maximum clock frequency	$\overline{PE}$ mode	Waveform 1	120	130		110		MHz
		Toggle mode		100	115		90		
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4.0 4.0	6.5 6.5	9.5 9.0	4.0 4.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_3$		Waveform 1	7.0 4.5	10.0 7.0	13.0 9.0	7.0 4.0	13.5 9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n		Waveform 2	5.0	7.5	10.5	5.0	11.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}_3$		Waveform 2	7.0	10.0	13.5	7.0	14.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Typ	Max	LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Max	UNIT
$t_s(H)$ $t_s(L)$	Setup time, High or Low J, $\overline{K}$ and D_n to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ and D_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	3.0 4.0			3.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns
$t_w(H)$	CP Pulse width High	Waveform 1	6.0			6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	6.0			6.0		ns

Document No.	853-1308
ECN No.	98907
Date of issue	February 23, 1990
Status	Product Specification
FAST Products	

FAST 74F219A

64-Bit TTL Bipolar RAM, Non-Inverting (3-State)

FEATURES

- **High speed performance**
- **Replaces 74F219**
- **Address access time: 8 ns max vs 28ns for 74F219**
- **Power dissipation: 4.3 mW/bit typ**
- **Schottky clamped TTL**
- **One chip enable**
- **Non-Inverting outputs (For inverting outputs see 74F189A)**
- **Buffered PNP inputs**
- **3-state outputs**
- **74F219A in 150 mil wide S.O. is preferred option for new designs**
- **C3F219A in 300 mil wide S.O.L. replaces 74F189 in existing designs**

APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F219A	5ns	55mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V\pm10\%$; $T_A = 0°C$ to $+70°C$
16-Pin Plastic DIP	N74F219AN
16-Pin Plastic SO (150 mil)	N74F219AD
16-Pin Plastic SOL (300 mil)	C3F219AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

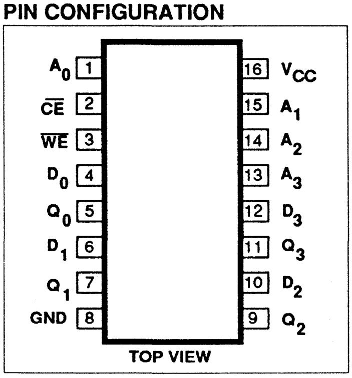
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Data inputs	1.0/1.0	20µA/0.6mA
$A_0 - A_3$	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Chip Enable input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{WE}$	Write Enable input (active Low)	1.0/2.0	20µA/1.2mA
$Q_0 - Q_3$	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

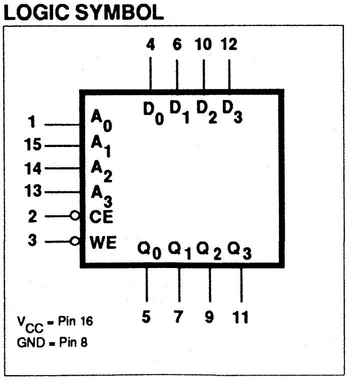
DESCRIPTION

The 74F219A is a high speed, 64-Bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are in High impedance state whenever the Chip Enable ($\overline{CE}$) is High. The outputs are active only in the READ mode ($\overline{WE}$ = High) and the output data is the same polarity as the stored data.

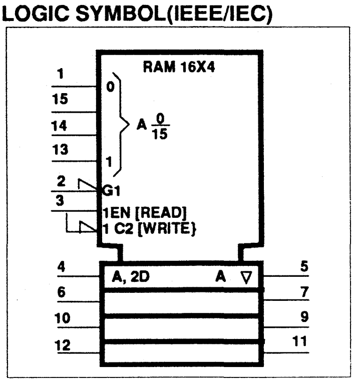
PIN CONFIGURATION



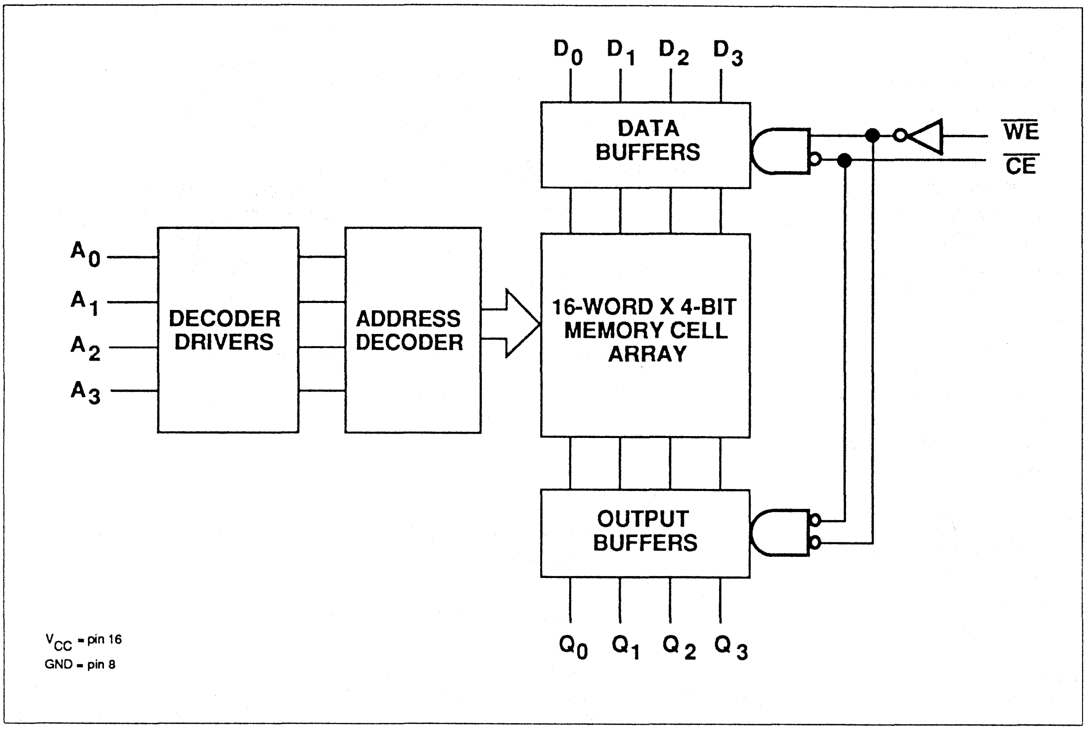
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
$\overline{CE}$	$\overline{WE}$	D_n	Q_n	
L	H	X	Stored data	Read
L	L	L	High impedance	Write "0"
L	L	H	High impedance	Write "1"
H	X	X	High impedance	Disable Input

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CE}$, $\overline{WE}$					-1.2	mA
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	mA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V				-50	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, $\overline{CE}$ = $\overline{WE}$ = GND			55	80	mA
C_{IN}	Input capacitance		V_{CC} = 5V, V_{IN} = 2.0V			4		pF
C_{OUT}	Output capacitance		V_{CC} = 5V, V_{OUT} = 2.0V			7		pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

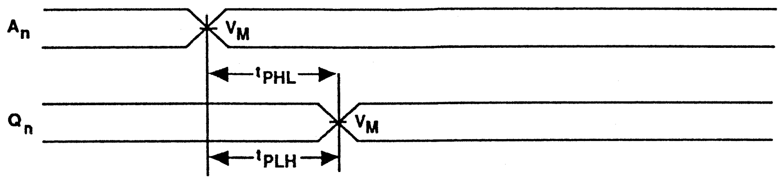
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Access time	Propagation delay A_n to $\overline{Q}_n$	Waveform 1	2.5 2.0	5.0 4.5	8.0 8.0	2.5 2.0	8.0 8.0	ns
t_{PZH} t_{PZL}	Access time	Enable time $\overline{CE}$ to $\overline{Q}_n$	Waveform 2	1.5 2.5	3.0 4.0	6.0 7.0	1.5 2.0	6.5 7.5	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{CE}$ to $\overline{Q}_n$		Waveform 3	2.5 1.5	4.5 3.0	7.0 5.5	2.0 1.0	8.0 6.0	ns
t_{PZH} t_{PZL}	Write recovery time	Enable time $\overline{WE}$ to $\overline{Q}_n$	Waveform 4	2.0 3.0	3.5 4.5	6.5 7.5	1.5 2.5	7.0 8.0	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{WE}$ to $\overline{Q}_n$		Waveform 4	3.0 1.5	5.0 3.5	8.0 6.0	2.5 1.5	9.0 7.0	ns

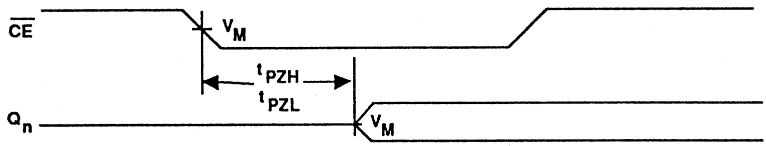
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time A_n to $\overline{WE}$	Waveform 4	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time A_n to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time D_n to $\overline{WE}$	Waveform 4	8.0 7.5			9.0 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_s(L)$	Setup time $\overline{CE}$ (falling edge) to $\overline{WE}$ (falling edge)	Waveform 4	0			0		ns
$t_h(L)$	Hold time $\overline{WE}$ (falling edge) to $\overline{CE}$ (rising edge)	Waveform 4	6.5			7.5		ns
$t_w(L)$	Pulse width, Low $\overline{WE}$	Waveform 4	7.0			8.0		ns

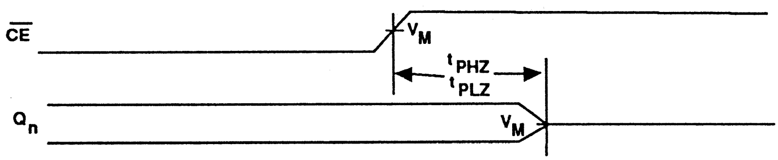
AC WAVEFORMS



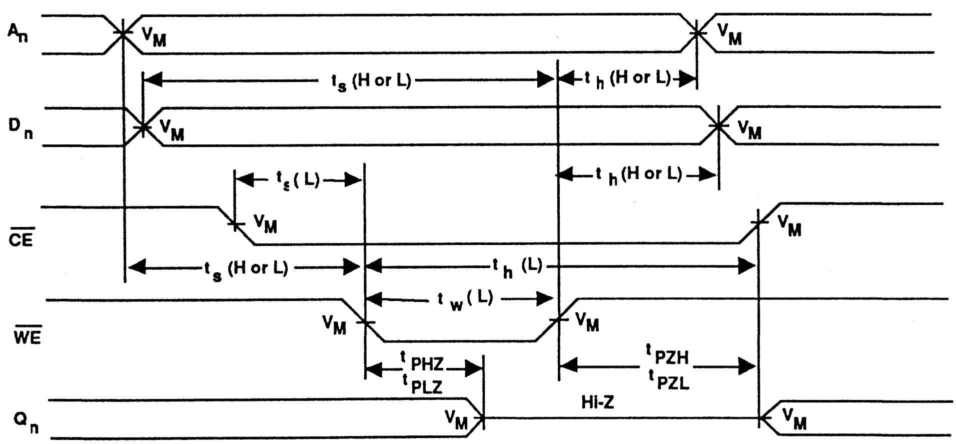
Waveform1. Read Cycle, Address Access Time



Waveform 2. Read Cycle, Chip Enable Access Time



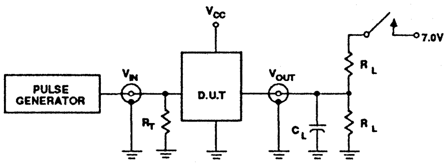
Waveform 3. Read Cycle, Chip Disable Time



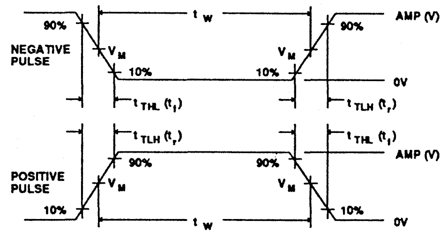
Waveform 4. Write Cycle

NOTES: 1. For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0356
ECN No.	98173
Date of issue	November 27, 1989
Status	Product Specification
FAST Products	

FAST 74F242, 74F243

Transceivers

74F242 Quad Transceiver, Inverting (3-State)
74F243 Quad Transceiver (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F242	4.3ns	31.2mA
74F243	4.0ns	66mA

ORDERING INFORMATION

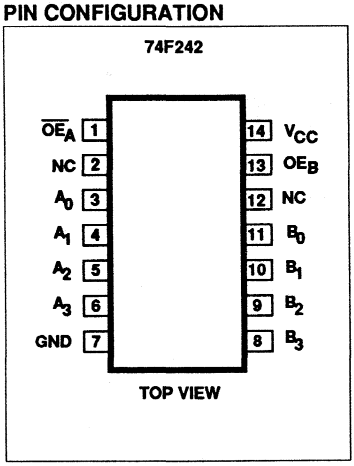
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F242N, N74F243N
14-Pin Plastic SO	N74F242D, N74F243D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

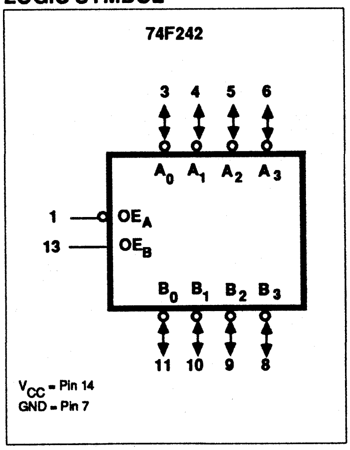
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_n, B_n	Data inputs ('F242)	3.5/1.67	70μA/1.0mA
A_n, B_n	Data inputs ('F243)	3.5/2.67	70μA/1.6mA
$\overline{OE}_A$	Output enable input (active Low)	1.0/1.67	20μA/1.0mA
OE_B	Output enable input	1.0/1.67	20μA/1.0mA
A_n, B_n	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

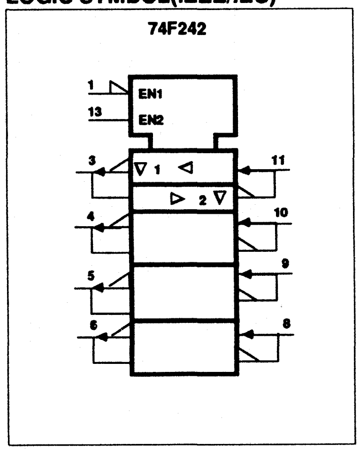
PIN CONFIGURATION



LOGIC SYMBOL



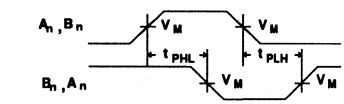
LOGIC SYMBOL(IEEE/IEC)



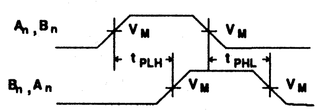
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	74F242	Waveform 1	2.5 2.0	3.5 3.0	6.0 4.5	2.5 2.0	7.0 4.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	74F242	Waveform 3 Waveform 4	3.0 3.5	4.0 6.5	7.0 9.0	3.0 3.5	8.0 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	74F242	Waveform 3 Waveform 4	3.5 3.5	5.5 6.0	8.5 9.5	3.5 3.5	9.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	74F243	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.2 6.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	74F243	Waveform 3 Waveform 4	2.0 2.0	4.5 5.0	5.7 7.5	2.0 2.0	6.7 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	74F243	Waveform 3 Waveform 4	2.0 2.0	4.0 4.5	6.0 6.0	2.0 2.0	7.0 7.0	ns

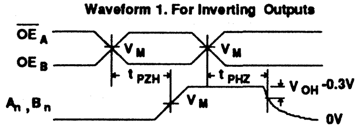
AC WAVEFORMS



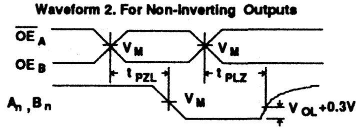
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



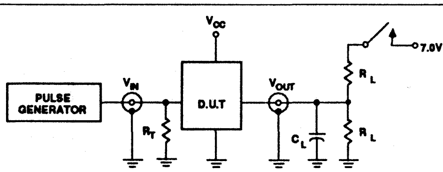
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

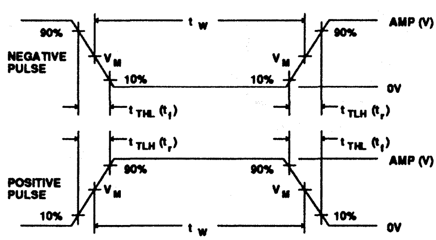
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0357
ECN No.	98769
Date of issue	February 8, 1990
Status	Product Specification
FAST Products	

FAST 74F244

Buffer

74F244 Octal Buffer (3-State)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F244	4.0ns	53mA

FEATURES

- **Octal bus interface**
- **3-State Output buffer output sink 64mA**
- **15mA source current**
- **Industrial temperture range available (-40°C to +85 °C)**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
20-Pin Plastic DIP	N74F244N	I74F244N
20-Pin Plastic SOL	N74F244D	I74F244D

DESCRIPTION

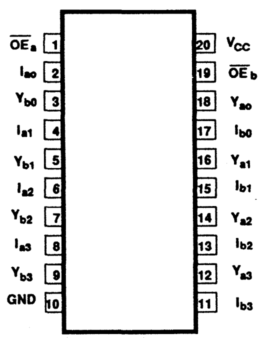
The 74F244 is an octal buffer that is ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_a$ and $\overline{OE}_b$, each controlling four of the 3-state outputs.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

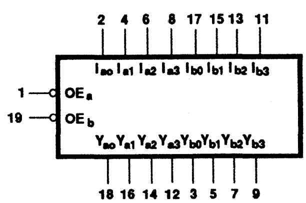
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/2.67	20μA/1.6mA
$\overline{OE}_a$ $\overline{OE}_b$	Output enable inputs (active Low)	1.0/1.67	20μA/1.0mA
Y_{an}, Y_{bn}	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

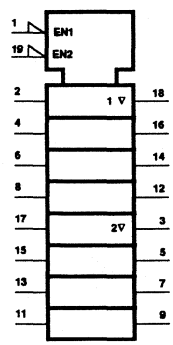


LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

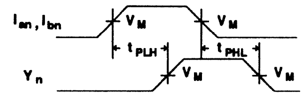
LOGIC SYMBOL(IEEE/IEC)



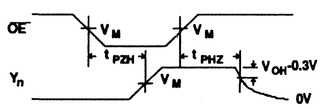
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		$T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	Waveform 1	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.2 6.5	1.5 2.0	7.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	2.0 2.0	4.3 5.0	5.7 7.0	2.0 2.0	6.7 8.0	2.0 2.0	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 2 Waveform 3	1.5 1.5	2.5 2.5	5.5 5.5	1.0 1.0	6.0 5.5	1.0 1.0	6.0 5.5	ns

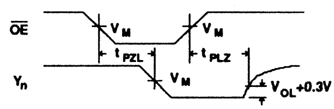
AC WAVEFORMS



Waveform 1. For Non-Inverting Outputs



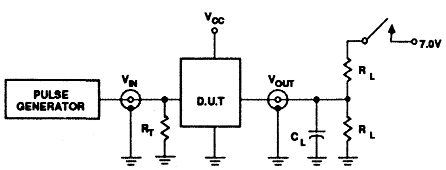
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

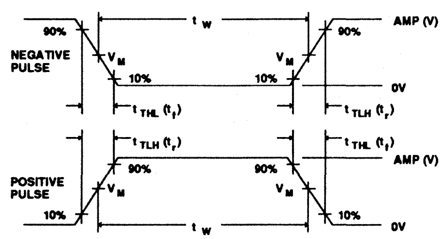
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0358
ECN No.	99143
Date of issue	March 19, 1990
Status	Product Specification
FAST Products	

FAST 74F251, 74F251A
Multiplexers

74F251 8-Input Multiplexer (3-State)
74F251A 8-Input Multiplexer (3-State)

FEATURES

- **High speed 8-to-1 multiplexing**
- **On chip decoding**
- **Multifunction capability**
- **Inverting and Non-Inverting outputs**
- **Both outputs are 3-state for further multiplexer expansion**

DESCRIPTION

The 74F251 and 74F251A are logic implementation of a single 8-position switch with the switch position controlled by the state of three Select (S_0,S_1,S_2) inputs. True(Y) and complementary ($\overline{Y}$) outputs are both provided. The output Enable ($\overline{OE}$) is active Low. When $\overline{OE}$ is High, both outputs are in high impedance state, allowing multiple output connections to a common bus without driving nor loading the bus significantly. All but one device must be in high impedance state to avoid high currents that would exceed the maximum ratings when the outputs of the 3-state devices are tied together. When the output of more than one device is tied together the user must ensure that there is no overlap in the active Low portion of the output enable voltages.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F251	5.5ns	15mA
74F251A	4.5ns	19mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F251N, N74F251AN
16-Pin Plastic SO	N74F251D, N74F251AD

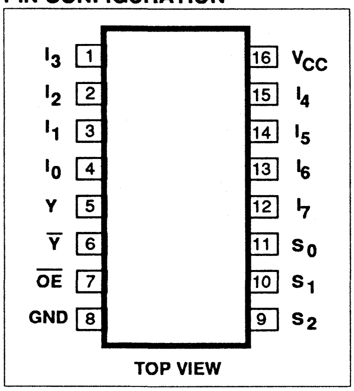
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0 - I_7	Data inputs	1.0/1.0	20μA/0.6mA
S_0 - S_2	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20μA/0.6mA
Y, $\overline{Y}$	Data outputs	150/40	3mA/24mA

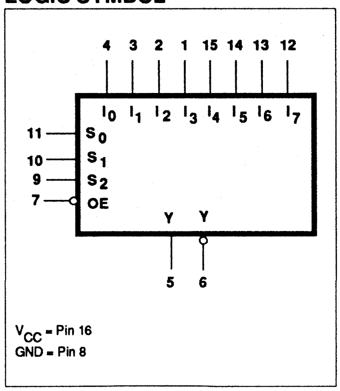
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

74F251A is the faster version of 74F251.

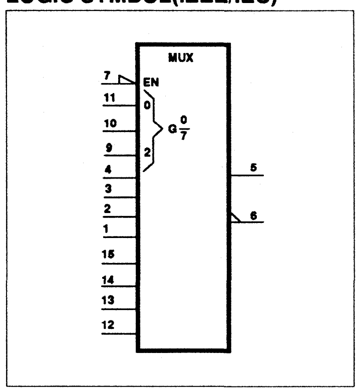
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	74F251	Waveform 2	3.0 3.0	4.0 4.5	6.0 6.5	2.5 3.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	74F251	Waveform 1	2.5 1.0	4.0 2.0	6.0 4.0	2.0 1.0	7.0 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	74F251	Waveform 1, 2	4.0 4.0	7.0 7.0	9.5 9.0	3.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	74F251	Waveform 1, 2	3.5 1.5	6.0 5.0	9.0 7.5	3.5 1.5	10.0 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Y	74F251	Waveform 3 Waveform 4	4.0 4.0	6.5 5.5	10.0 8.0	4.0 3.5	11.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Y	74F251	Waveform 3 Waveform 4	2.5 3.0	4.0 4,0	6.5 6.5	2.0 2.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to $\overline{Y}$	74F251	Waveform 3 Waveform 4	4.0 4.0	5.5 5.5	8.0 8.0	3.5 3.5	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to $\overline{Y}$	74F251	Waveform 3 Waveform 4	2.5 2.0	4.0 4.0	6.0 6.5	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y	74F251A	Waveform 2	3.0 3.0	5.0 5.0	7.0 7.0	2.5 3.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	74F251A	Waveform 1	2.5 1.0	4.5 2.5	7.0 5.0	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	74F251A	Waveform 1, 2	4.5 4.0	6.5 5.5	10.0 9.0	4.0 3.5	11.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	74F251A	Waveform 1, 2	3.5 2.5	6.0 4.5	9.0 7.0	3.5 2.5	9.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Y	74F251A	Waveform 3 Waveform 4	3.5 3.5	5.5 5.0	7.5 7.5	3.0 3.0	8.5 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Y	74F251A	Waveform 3 Waveform 4	2.5 1.0	4.0 4.0	6.5 6.0	2.0 1.0	7.0 6.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to $\overline{Y}$	74F251A	Waveform 3 Waveform 4	2.5 2.5	4.0 4.0	6.5 6.5	2.0 2.5	7.0 7.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to $\overline{Y}$	74F251A	Waveform 3 Waveform 4	3.5 1.0	5.0 2.0	7.5 4.5	3.0 1.0	8.0 4.5	ns

Document No.	853-0360
ECN No.	98483
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F257, 74F257A

Data Selectors/Multiplexers

74F257 Quad 2-Line To 1-Line Selector/Multiplexer, Non-Inverting (3-State)
74F257A Quad 2-Line To 1-Line Selector/Multiplexer, Non-Inverting (3-State)

FEATURES

- **Multifunction capability**
- **Non-inverting data path**
- **3-state outputs**
- **See 'F258A for inverting version**

DESCRIPTION

The 74F257/74F257A has four identical 2-input multiplexers with 3-state outputs which select 4 bits of data from two sources under control of a common Select (S) input. The I_{0n} inputs are selected when the common Select input is Low and the I_{1n} inputs are selected when the common Select input is High. Data appears at the outputs in true non-inverted form from the selected inputs.The 'F257/'F257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the common Select input. Outputs are forced to a high impedance "off" state when the Output Enable ($\overline{OE}$) is High. All but one device must be in high impedance state to avoid currents that would exceed the maximum ratings if the outputs were tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-state devices were tied together.

The 74F257A is the faster version of 74F257.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F257	4.3ns	12mA
74F257A	4.3ns	12mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F257N, N74F257AN
16-Pin Plastic SO	N74F257D, N74F257AD

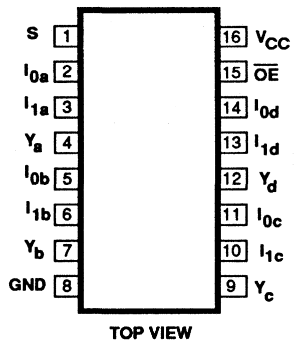
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}, I_{1n}	Data inputs	1.0/1.0	20μA/0.6mA
S	Common Select input	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{Y}_a$ - $\overline{Y}_d$	Data outputs	150/33	3.0mA/20mA

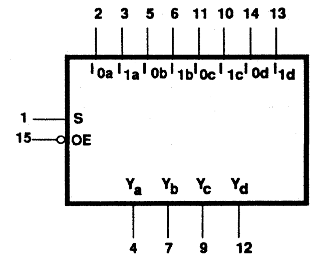
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

Data Selectors/Multiplexers FAST 74F257, 74F257A

PIN CONFIGURATION

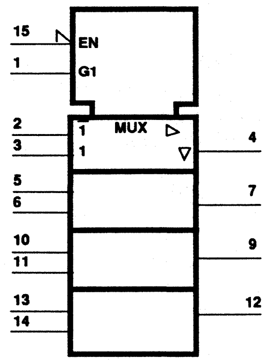


LOGIC SYMBOL

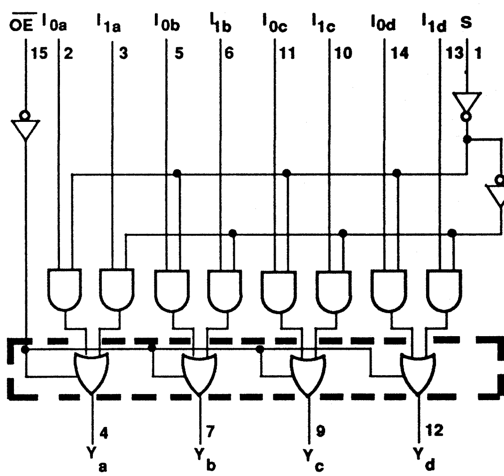


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Document No.	853-0056
ECN No.	98778
Date of issue	February 9, 1990
Status	Product Specification
FAST Products	

FAST 74F269 Counter

8-Bit Bidirectional Binary Counter

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F269	115MHz	95mA

FEATURES

- **Synchronous counting and loading**
- **Built-in look-ahead carry capability**
- **Count frequency 115 MHz typ**
- **Supply current 95mA typ**

DESCRIPTION

The 74F269 is a fully synchronous 8-stage Up/Down Counter featuring a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

ORDERING INFORMATION

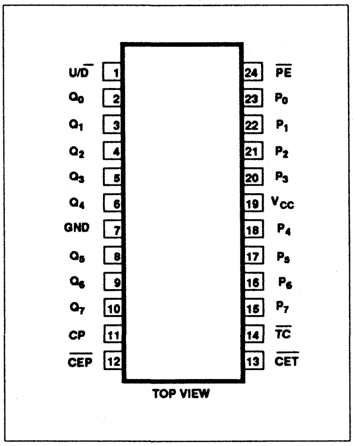
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim Dip (300 mil)	N74F269N
24-Pin Plastic SOL	N74F269D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

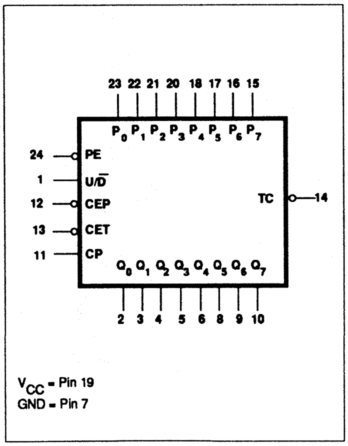
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
P_0 - P_7	Parallel Data inputs	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable Parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal Count output (active Low)	50/33	1.0mA/20mA
Q_0 - Q_7	Flip-flop outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

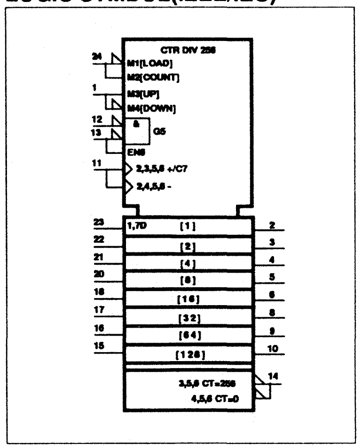
PIN CONFIGURATION



LOGIC SYMBOL

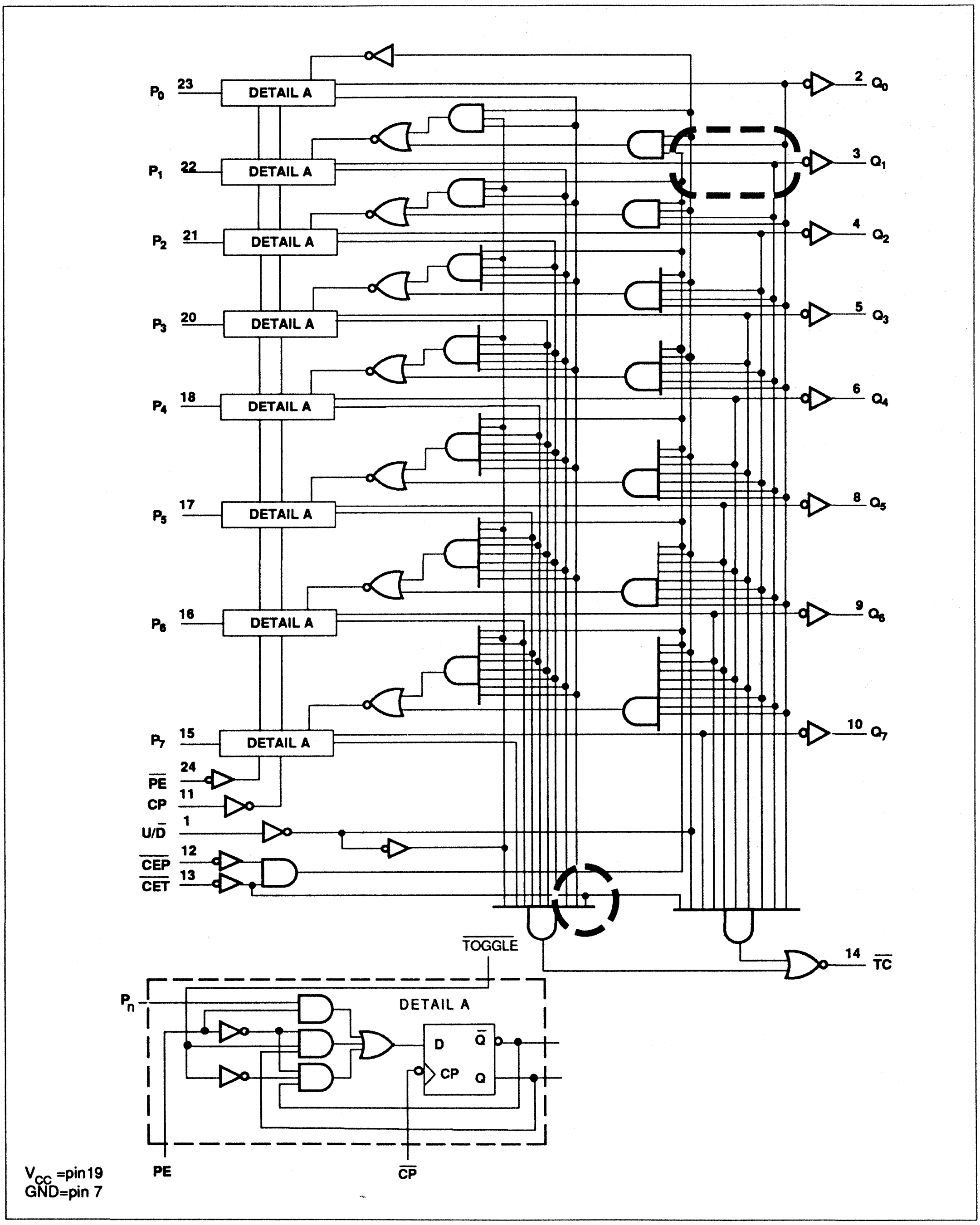


LOGIC SYMBOL(IEEE/IEC)



Counter FAST 74F269

LOGIC DIAGRAM



MODE SELECT-FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	P_n	Q_n	$\overline{TC}$	
↑ ↑	X X	X X	X X	l l	l h	L H	(a) (a)	Parallel load
↑	h	l	l	h	X	Count up	(a)	Count up
↑	l	l	l	h	X	Count down	(a)	Count down
↑ ↑	X X	h X	l h	h h	X X	q_n q_n	(a) H	Hold (do nothing)

H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(a) = $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. The Terminal Count up is with all Q_n outputs High andTerminal Count Down is with all Q_n outputs Low.

APPLICATION

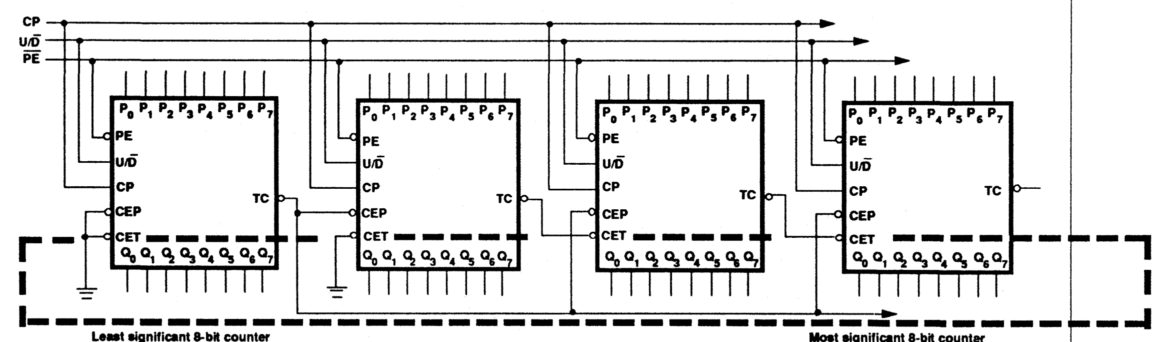


Figure 1
Synchronous multistage counting scheme

Document No.	853-0363
ECN No.	99142
Date of issue	March 19 1990
Status	Product Specification
FAST Products	

FAST 74F280A, 74F280B

Parity Checker Generator

9-Bit Odd/Even Parity Generator/Checker

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F280A	6.5ns	26mA
74F280B	5.5ns	26mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in Low and High states)**
- **Buffered inputs--one normalized load**
- **Word length easily expanded by cascading**
- **Industrial temperature range available (-40°C to +85°C) for 74F280B**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
14-Pin Plastic DIP	N74F280AN, N74F280BN	I74F280BN
14-Pin Plastic SO	N74F280AD, N74F280BD	I74F280BD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0-I_8	Data inputs	1.0/0.033	20μA/20μA
Σ_E , Σ_O	Parity outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

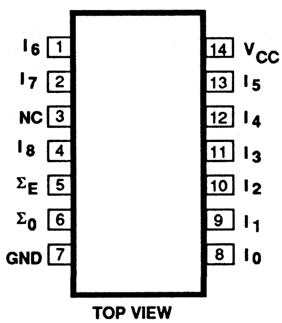
The 74F280A is a 9-bit Parity Generator or Checker commonly used to detect errors in high speed data transmission or data retreival systems. Both Even (Σ_E) and Odd (Σ_O) parity outputs are available for generating and checking even or odd parity on up to 9 bits.

The Even (Σ_E) parity output is High when an even number of data inputs (I_0-I_8) are High. The Odd (Σ_O) parity output is High when an odd number of data inputs are High.

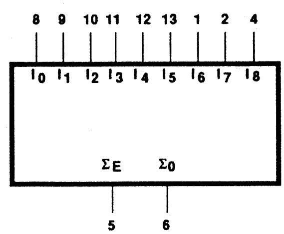
Expansion to larger word sizes is accomplished by tying the Even (Σ_E) outputs of up to nine parallel devices to the data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 20 ns.

The 74F280B is a faster version of 74F280A

PIN CONFIGURATION

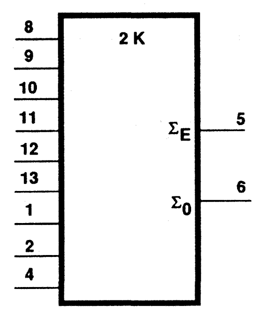


LOGIC SYMBOL



V_{CC} =Pin 14
GND=Pin 7

LOGIC SYMBOL(IEEE/IEC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	-40		85	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

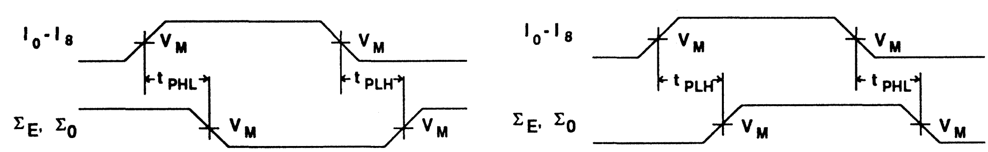
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
	Input clamp voltage		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input current at maximum input voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I			V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current	Commercial range	V_{CC} = MAX, V_I = 2.7V				20	µA
	Low-level input current	Industrial range					40	µA
I_{IL}	Short-circuitoutput current[3]		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_{OS}	Supply current (total)		V_{CC} = MAX		-60		-150	mA
I_{CC}			V_{CC} = MAX			26	35	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS: $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		$T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_E	'F280A	Waveform 1,2	5.0 7.5	7.0 10.0	9.0 13.0	5.0 7.5	10.0 14.5			ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_O	'F280A	Waveform 1,2	6.5 7.0	8.6 9.1	10.5 12.0	6.5 6.0	11.0 13.0			ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_E	'F280B	Waveform 1,2	4.0 4.0	6.5 7.0	9.0 10.0	3.5 3.5	10.0 11.1	3.0 3.5	11.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_O	'F280B	Waveform 1,2	4.0 4.0	6.5 7.0	9.0 10.0	3.5 3.5	10.0 11.0	3.0 3.5	11.0 12.0	ns

AC WAVEFORMS

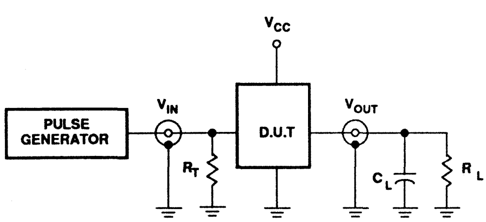


Waveform 1. Propagation Delay For Inverting Outputs

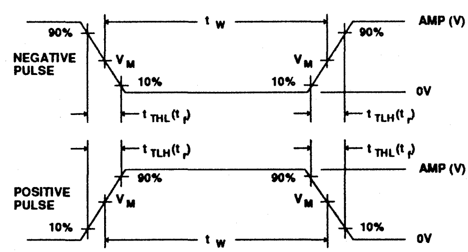
Waveform 2. Propagation Delay For Non-Inverting Outputs

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0061
ECN No.	97377
Date of issue	August 14, 1989
Status	Product Specification
FAST Products	

FAST 74F298
Multiplexer

Quad 2-Input Multiplexer With Storage

FEATURES

- **Fully synchronous operation**
- **Select from two data sources**
- **Buffered, negative edge triggered clock**
- **Provides the equivalent of function capabilities of two separate MSI functions (74F157 and 74F175)**

DESCRIPTION

The 74F298 is a high speed Quad 2-Input Multiplexer with storage. It selects 4 bits of data from two sources (ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the High-to-Low transition of the clock ($\overline{CP}$). The 4-bit register is fully edge triggered. The data inputs (I_0 and I_1) and Select input (S) must be stable only one setup time prior to the High-to-Low transition of the clock for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F298	115MHz	30mA

ORDERING INFORMATION

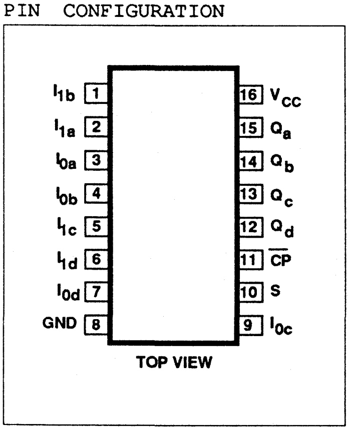
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-pin Plastic DIP	N74F298N
16-pin Plastic SO	N74F298D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

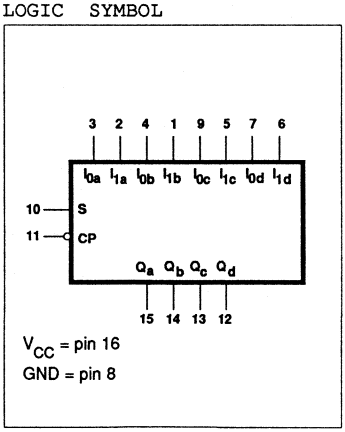
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}, I_{0b}, I_{0c}, I_{0d}	Data inputs	1.0/1.0	20µA/0.6mA
I_{1a}, I_{1b}, I_{1c}, I_{1d}	Data inputs	1.0/1.0	20µA/0.6mA
S	Select input	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock input (active falling edge)	1.0/1.0	20µA/0.6mA
Q_a, Q_b, Q_c, Q_d	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

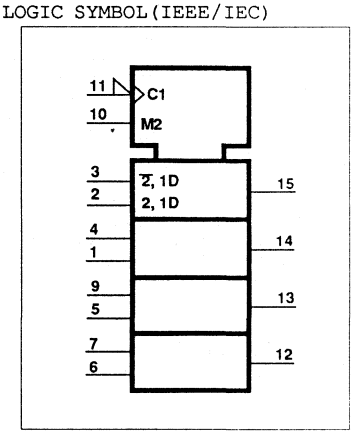
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS Min	Nom	Max	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS Min	Typ[2]	Max	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=-MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuitoutput current[3]	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX				30	40	mA
	I_{CCL}					32	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	110	115		105		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n	Waveform 1	4.0 4.5	5.5 6.5	7.5 8.5	4.0 4.5	9.0 9.5	ns

Document No.	853-0365
ECN No.	98989
Date of issue	March 1, 1990
Status	Product Specification
FAST Products	

FAST 74F299

Register

8-Bit Universal Shift/Storage Register(3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F299	115 MHz	58mA

FEATURES

- **Common parallel I/O for reduced pin count**
- **Additional serial inputs and outputs for expansion**
- **Four operating modes: Shift left, shift right, load and store**
- **3-state outputs for bus oriented applications**

DESCRIPTION

The 74F299 is an 8-bit universal shift / storage register with 3-state outputs. Four modes of operation are possible: Hold (store), shift left, shift right and parallel load. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active-Low Master Reset is used to reset the register.

The 74F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous, shift left, shift right, parallel

ORDERING INFORMATION

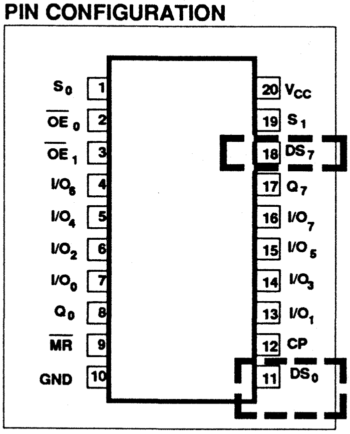
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F299N
20-Pin Plastic SOL	N74F299D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

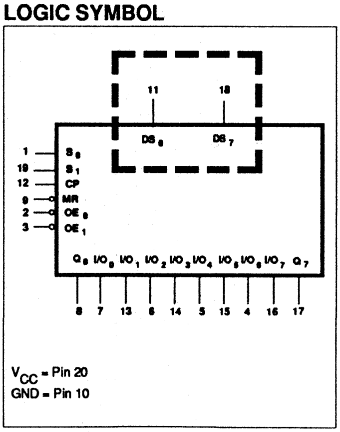
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
DS_0	Serial data input for right shift	1.0/1.0	20μA/0.6mA
DS_7	Serial data input for left shift	1.0/1.0	20μA/0.6mA
S_0, S_1	Mode Select inputs	1.0/2.0	20μA/1.2mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{OE}_0, \overline{OE}_1$	Output Enable input (active Low)	1.0/1.0	20μA/0.6mA
Q_0, Q_7	Serial outputs	50/33	1.0mA/20mA
I/O_n	Multiplexed parallel data inputs or	3.5/1.0	70μA/0.6mA
	3-state parallel outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

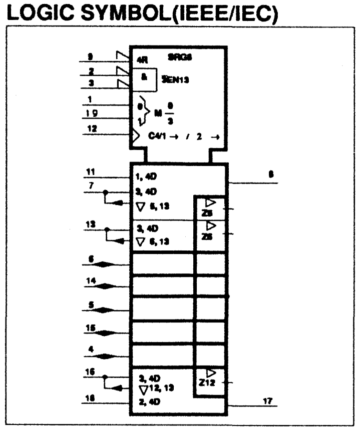
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

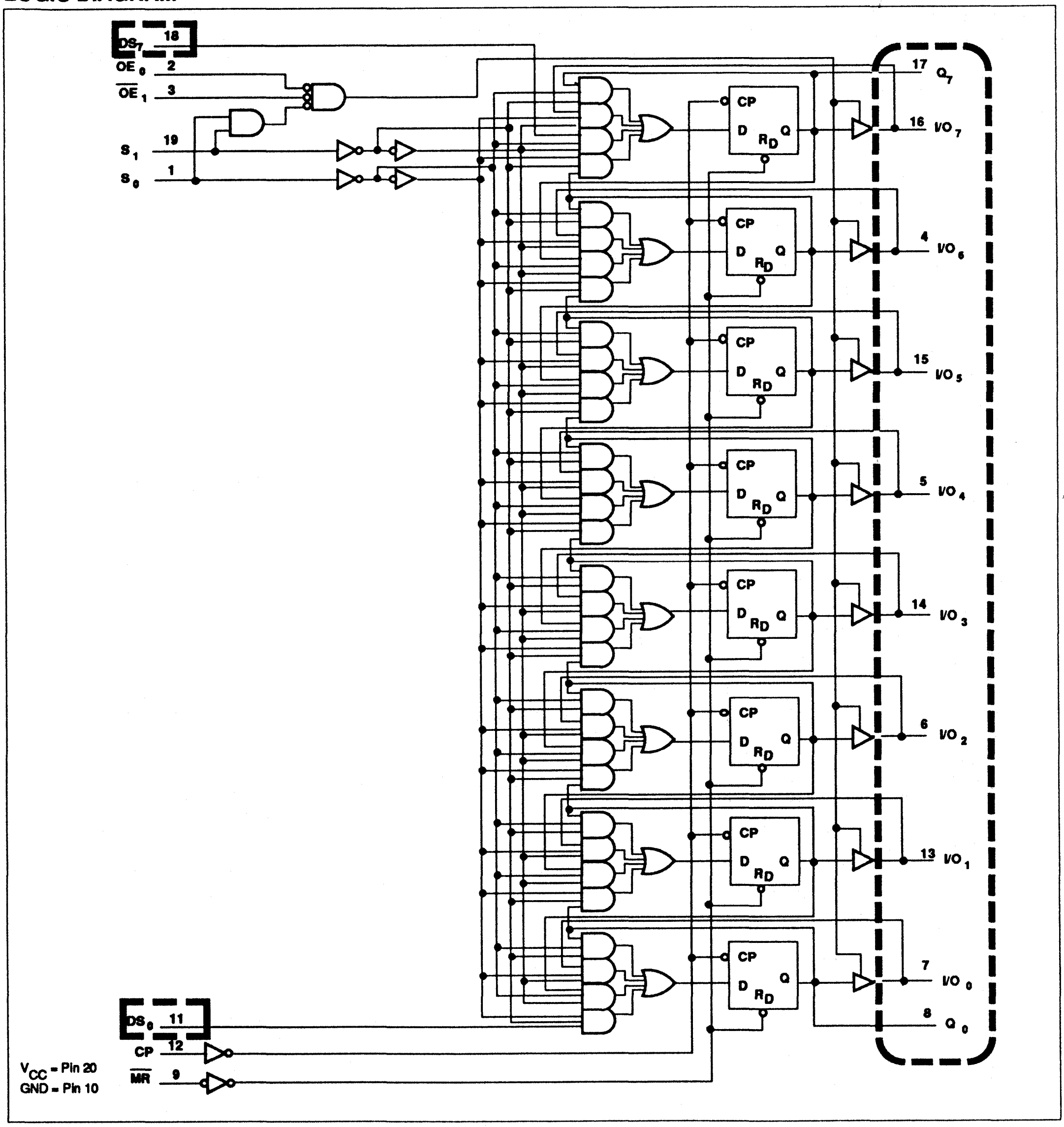


DESCRIPTION (Continued)

load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Function Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting on longer words. A Low signal on $\overline{MR}$ overrides the Select and and CP input and resets the flip-flops.

All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended set up and hold times, relative to the rising edge of clock are observed. A High signal on either $\overline{OE}_0$ or $\overline{OE}_1$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by High signals on both S_0 and S_1 in preparation for a parallel load operation.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{OE}_n$	$\overline{MR}$	S_1	S_0	CP	
L	L	X	X	X	Asynchronous Reset; Q_0-Q_7=Low
L	H	H	H	↑	Parallel load ; $I/O_n \rightarrow Q_n$ (I/O_n outputs disabled)
L	H	L	H	↑	Shift right ; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
L	H	H	L	↑	Shift left ; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
L	H	L	L	X	Hold
H	X	X	X	X	Outputs in High Z

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	Q_0, Q_7	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_0, Q_7			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	Q_0, Q_7			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

Document No.	853-0367
ECN No.	98987
Date of issue	March 1, 1990
Status	Product Specification
FAST Products	

FAST 74F323

Register

8-Bit Universal Shift/Storage Register With Synchronous Reset and Common I/O pins (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F323	115 MHz	55mA

FEATURES

- **Common parallel I/O for reduced pin count**
- **Additional serial inputs and outputs for expansion**
- **Four operating modes: Shift left, shift right, load and store**
- **3-state outputs for bus oriented applications**

DESCRIPTION

The 74F323 is an 8-bit universal shift /storage register with 3-state outputs.Its function is similar to the 74F299 with the exception of synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin counts. Separate serial inputs and outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. Four modes of operation are possible: Hold (store), shift left, shift right and parallel load.

The 74F323 contains eight edge-triggered D-type flip-flops and the interstage logic

ORDERING INFORMATION

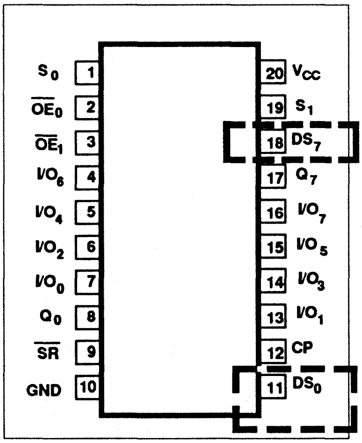
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F323N
20-Pin Plastic SOL	N74F323D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

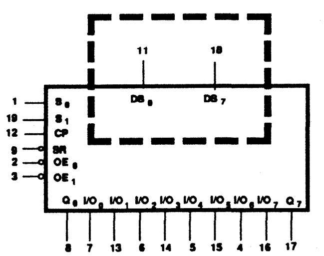
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
DS_0	Serial data input for right shift	1.0/1.0	20µA/0.6mA
DS_7	Serial data input for left shift	1.0/1.0	20µA/0.6mA
S_0 ,S_1	Mode select inputs	1.0/2.0	20µA/1.2m
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$,$\overline{OE}_1$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
Q_0 ,Q_7	Serial outputs	50/33	20µA/20mA
I / O_n	Multiplexed parallel data inputs or	3.5/1.0	70µA/0.6mA
	3-state parallel outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

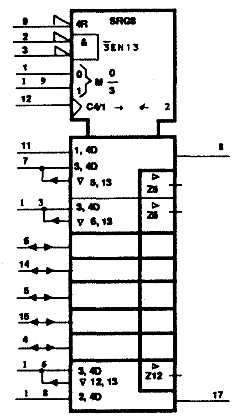


LOGIC SYMBOL



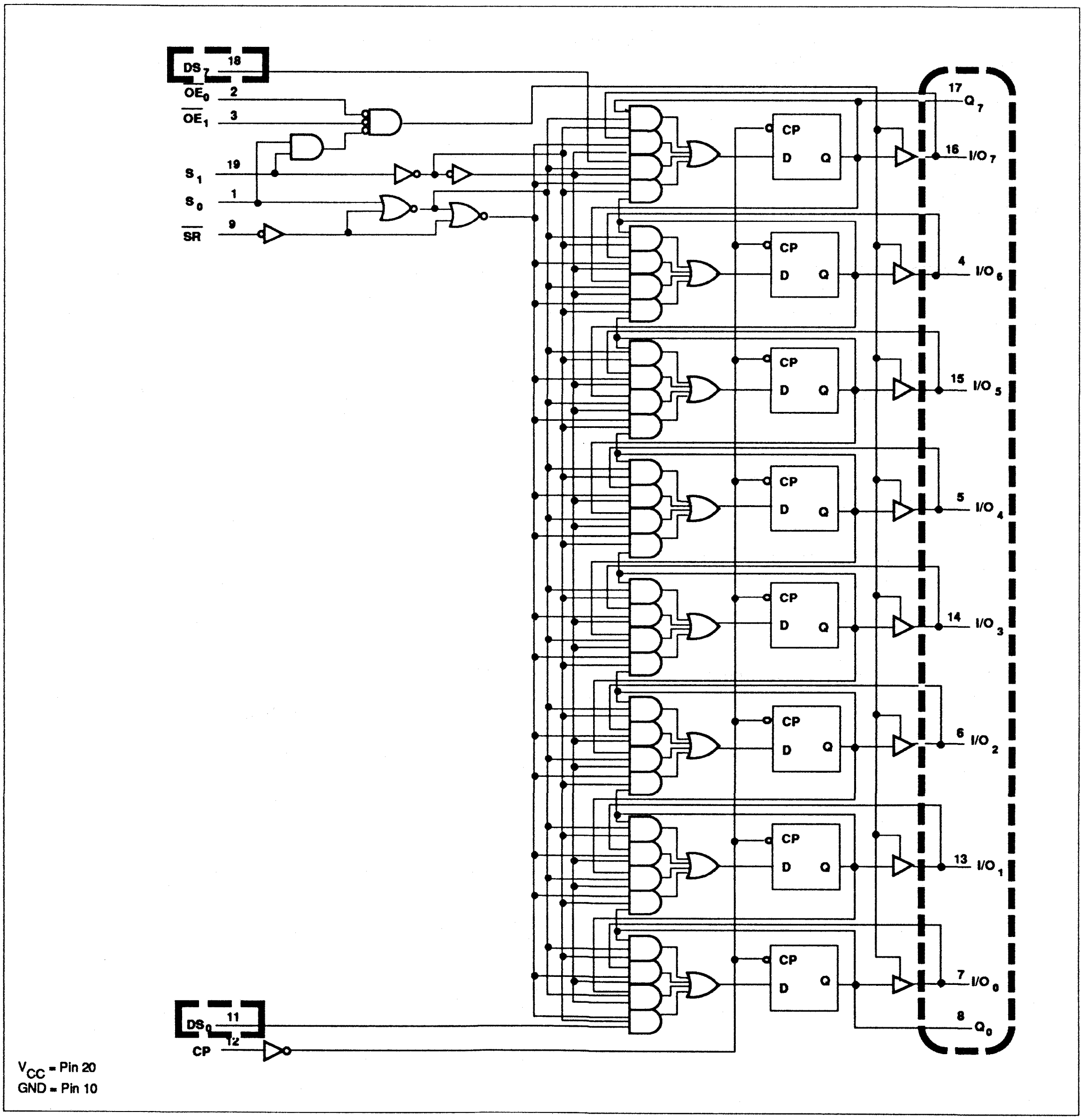
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operations is determined by S_0 and S_1, as shown in the Function Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words. A Low signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of clock. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended set up and hold times, relative to the rising edge of clock are observed. A high signal on either $\overline{OE}_0$ or $\overline{OE}_1$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by High signals on both S_0 and S_1 in preparation for a parallel load operation.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{OE}_n$	$\overline{SR}$	S_1	S_0	CP	
L	L	X	X	↑	Synchronous Reset; Q_0-Q_7=Low
L	H	H	H	↑	Parallel load ; $I/O_n \rightarrow Q_n$
L	H	L	H	↑	Shift right ; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc
L	H	H	L	↑	Shift left ; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
L	H	L	L	X	Hold
H	X	X	X	X	Outputs disabled (3-state)

H = High voltage level
L = Low voltage level
NC = No change
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Q_0, Q_7	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_0, Q_7			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	Q_0, Q_7			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

Document No.	853-0042
ECN No.	98496
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F365, 74F366 74F367, 74F368 Buffers/Drivers

'F365, 'F367 Hex Buffer/Driver (3-State)
'F366, 'F368 Hex Inverter Buffer/Driver (3-State)

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **High speed**
- **Bus oriented**
- **3-state buffer outputs sink 64mA**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F365, 74F367	5.0ns	36mA
74F366, 74F368	5.0ns	33mA

ORDERING INFORMATION

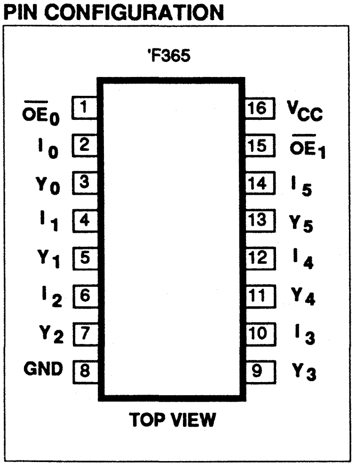
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F365N, N74F366N, N74F367N, N74F368N
16-Pin Plastic SO	N74F365D, N74F366D, N74F367D, N74F368D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

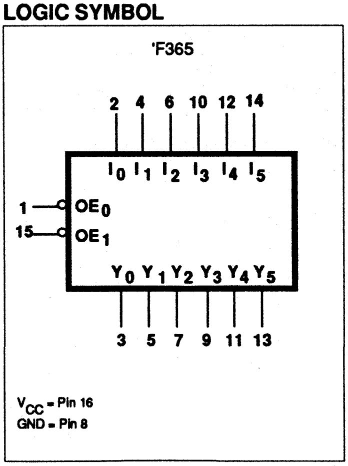
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0-I_5	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$,$\overline{OE}_1$	Output enable inputs (active Low)	1.0/0.033	20μA/20μA
Y_0- Y_5, $\overline{Y}_0$- $\overline{Y}_5$	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

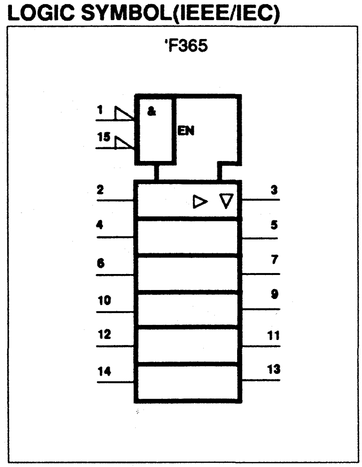
PIN CONFIGURATION



LOGIC SYMBOL



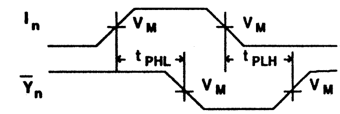
LOGIC SYMBOL(IEEE/IEC)



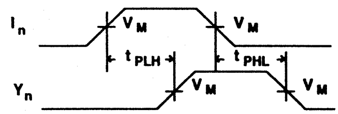
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	'F366, 'F368	Waveform 1	3.0 2.0	5.0 3.0	6.5 5.0	3.0 1.5	7.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	'F365, 'F367	Waveform 2	2.5 2.5	4.5 5.5	6.5 7.0	2.0 2.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F365, 'F366	Waveform 3 Waveform 4	2.5 2.5	4.0 5.0	6.5 8.0	2.5 2.5	7.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F367, 'F368	Waveform 3 Waveform 4	3.0 3.0	5.5 6.5	7.5 8.5	3.0 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	6.5 6.5	2.0 2.0	7.0 7.0	ns

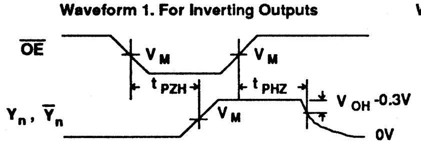
AC WAVEFORMS



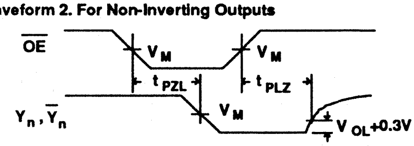
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



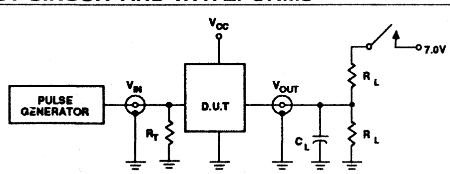
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M =1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

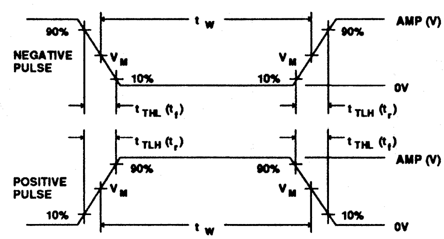
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0369
ECN No.	98488
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F373, 74F374

Latch/Flip-Flop

74F373 Octal Transparent Latch (3-State)
74F374 Octal D Flip-Flop (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F373	4.5ns	35mA

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F374	165MHz	55mA

FEATURES

- **8-bit transparent latch-'F373**
- **8-bit positive edge triggered register-'F374**
- **3-State Outputs glitch free during power-up and power-down**
- **Common 3-state Output register**
- **Independent register and 3-state buffer operation**

DESCRIPTION

The 74F373 is an octal transparent latch coupled to eight 3-State output devices. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High, and stores the data that is present one set-up time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs.

When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 'F374 is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is Low, the data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F373N, N74F374N
20-Pin Plastic SOL	N74F373D, N74F374D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.6mA
E ('F373)	Enable input (active High)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP ('F374)	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	3-State outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

Document No.	853-0067
ECN No.	97804
Date of issue	October 5, 1989
Status	Product Specification
FAST Products	

FAST 74F378
Flip-Flop

Hex D Flip-Flop With Enable

FEATURES

- 6-bit high-speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common Clock and Enable inputs
- Input clamp diodes limit high speed termination effects
- Fully TTL and CMOS compatible

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F378	100MHz	35mA

DESCRIPTION

The 74F378 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) input is Low.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output. The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

ORDERING INFORMATION

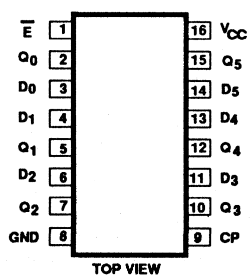
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F378N
16-Pin Plastic SO	N74F378D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

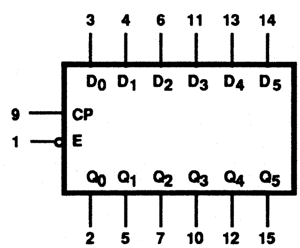
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_5$	Data inputs	1.0/1,0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1,0	20µA/0.6mA
$\overline{E}$	Enable input (active Low)	1.0/1,0	20µA/0.6mA
$Q_0 - Q_5$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

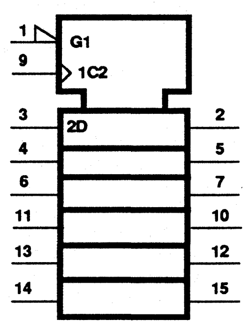


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



Document No.	853-1310
ECN No.	98498
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F410

Register Stack-16X4 RAM 3-State Output Register

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F410	19.5ns	45mA

FEATURES

- **Edge-triggered output register**
- **Typical access time of 19.5ns**
- **Optimize for register stack operation**
- **3-state outputs**
- **18-pin package**

DESCRIPTION

The 74F410 is a register oriented high speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge-triggered 4-bit output register allows new input data to be written while previous data is held. 3-state outputs are provided for maximum versatility. The 74F410 is fully compatible with all TTL families.

ORDERING INFORMATION

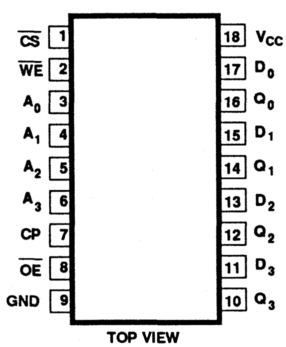
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
18-Pin Plastic DIP (300 mil wide)	N74F410N

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

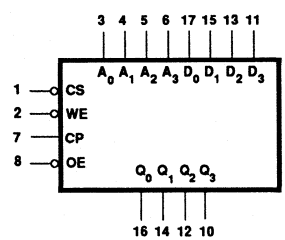
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Address inputs	1.0/1.0	20µA/0.6mA
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{WE}$	Write Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/2.0	20µA/1.2mA
Q_0 - Q_3	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

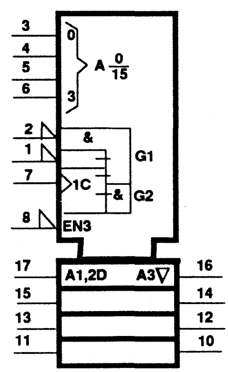


LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

LOGIC SYMBOL(IEEE/IEC)



Register Stack-16 X 4 RAM 3-State Output Register

FAST 74F410

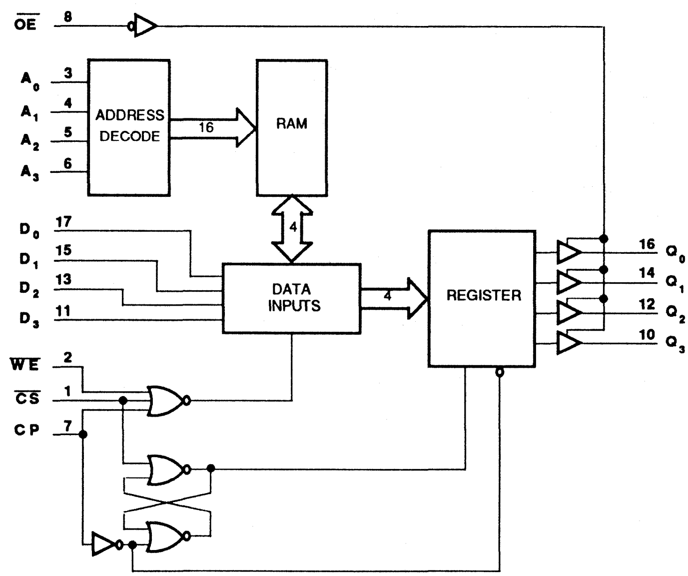
FUNCTIONAL DESCRIPTION

Write Operation--- When the three control inputs, Write Enable ($\overline{WE}$), Chip Select ($\overline{CS}$), and Clock (CP), are Low the information on the data inputs (D_0-D_3) is written into the memory location selected by the address inputs (A_0-A_3). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are Low, the contents of the selected memory location follow these changes, provided setup and hold time criteria are met.

Read Operation--- When $\overline{CS}$ is Low, $\overline{WE}$ is High, and CP goes from Low-to-High, the contents of the memory location selected by the address inputs (A_0-A_3) are edge-triggered into the Output Register.

When $\overline{WE}$ is Low, $\overline{CS}$ is Low, and CP goes from Low-to-High, the data at the Data inputs is edge-triggered into the Output Register. The $\overline{OE}$ input controls the output buffers. When $\overline{OE}$ is High the four outputs (Q_0-Q_3) are in a high impedance or OFF-state; when $\overline{OE}$ is Low, the outputs are determined by the state of the Output Register.

LOGIC DIAGRAM



V_{CC} = Pin 18
GND = Pin 9

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

Document No.	853-0373
ECN No.	97675
Date of issue	September 20, 1989
Status	Product Specification
FAST Products	

FAST 74F524

Comparator

8-Bit Register Comparator (Open Collector+3-State)

FEATURES

- **8-Bit bidirectional register with bus-oriented input-output**
- **Independent serial input-output to register**
- **Register bus comparator with 'equal to', 'greater than' and 'less than' outputs**
- **Cascadable in groups of 8-bits**
- **Open collector comparator outputs for AND-wired expansion**
- **Two's complement or magnitude compare**

DESCRIPTION

The 74F524 is an 8-bit bidirectional register with parallel input and output plus serial input and output progressing from LSB to MSB. All data inputs, serial and parallel, are loaded by the rising edge of the clock. The device functions are controlled by two control lines (S_0,S_1) to execute shift, load, hold and read out. An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-High, open collector outputs representing 'register equal to bus', 'register greater than bus' and 'register less than bus' are provided. These outputs can be disabled to the OFF state by the use of Status Enable ($\overline{SE}$). A mode control has also been provided to allow Two's Complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F524	65MHz	110mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F524N
20-Pin Plastic SOL[1]	N74F524D

NOTE:
1.Thermal mounting techniques are recommended.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/On	Parallel data inputs	3.5/1.0	70µA/0.6mA
S_0, S_1	Mode select inputs	1.0/1.0	20µA/0.6mA
C/SI	Status priority or serial data input	1.0/1.0	20µA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SE}$	Status enable input (active Low)	1.0/1.0	20µA/0.6mA
M	Compare mode select input	1.0/1.0	20µA/0.6mA
I/O_n	3-state parallel data outputs	150/40	3.0mA/24mA
C/SO	Status priority or serial data output	50/33	1.0mA/20mA
LT	Register less than bus output	OC/33	OC/20mA
EQ	Register equal to bus output	OC/33	OC/20mA
GT	Register greater than bus output	OC/33	OC/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

Document No.	853-1274
ECN No.	98905
Date of issue	Febnruary 23, 1990
Status	Product Specification
FAST Products	

FAST 74F539

Dual 1-Of-4 Decoder (3-state)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F539	7.5 ns	40mA

DESCRIPTION

The 74F539 contains two independent decoders. Each accepts two address (A_0 - A_1) input signals and decodes them to select one of four mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active Low (P=H) or active High (P=L). An active-Low Enable ($\overline{E}$) is available for data demultiplexing. Data is routed to the selected output in non-inverted or inverted form in the active-Low mode or inverted form in the active-High mode. A High signal on the Output Enable ($\overline{OE}_n$) input forces the 3-state outputs to the high impedance state.

ORDERING INFORMATION

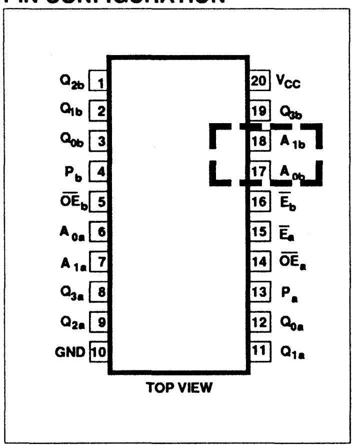
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F539N
20-Pin Plastic SOL	N74F539D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

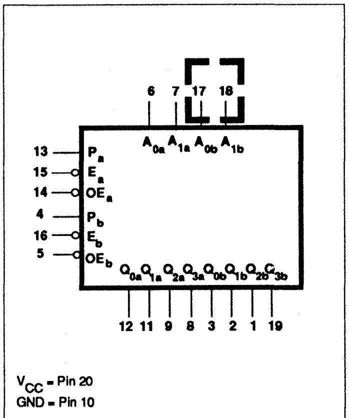
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_{0a}, A_{1a}	Decoder A Address inputs	1.0/1.0	20µA/0.6mA
A_{0b}, A_{1b}	Decoder B Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_a$, $\overline{E}_b$	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_a$, $\overline{OE}_b$	Output enable inputs (active Low)	1.0/1.0	20µA/0.6mA
P_a, P_b	Polarity control inputs	1.0/1.0	20µA/0.6mA
Q_{0a} - Q_{3a}	Decoder A Data outputs	150/40	3.0mA/24mA
Q_{0b} - Q_{3b}	Decoder B Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

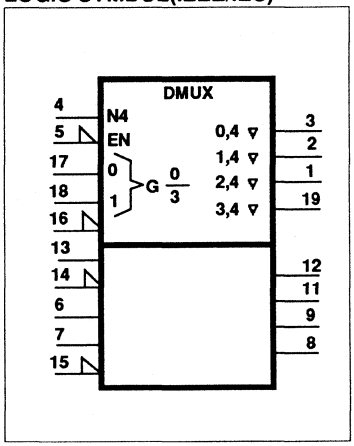


LOGIC SYMBOL

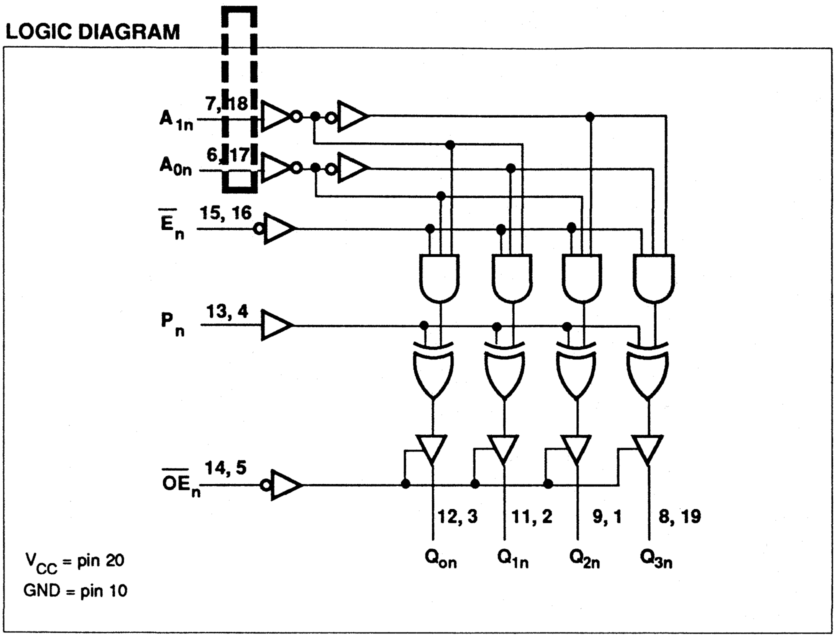


V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS				OPERATING MODE
$\overline{OE}_n$	$\overline{E}_n$	A_{1n}	A_{0n}	Q_{0n}	Q_{1n}	Q_{2n}	Q_{3n}	
H	X	X	X	Z	Z	Z	Z	High impedance
L	H	X	X	Q_n = P				Disable
L	L	L	L	H	L	L	L	Active High output (P=L)
L	L	L	H	L	H	L	L	
L	L	H	L	L	L	H	L	
L	L	H	H	L	L	L	H	
L	L	L	L	L	H	H	H	Active Low output (P=H)
L	L	L	H	H	L	H	H	
L	L	H	L	H	H	L	H	
L	L	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off "state.

Document No.	853-0068
ECN No.	98494
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F540, 74F541
Buffers

74F540 Octal Inverter Buffer (3-State)
74F541 Octal Buffer (3-State)

FEATURES

- **High impedance NPN base inputs for reduced loading (20µA in High and Low states)**
- **Low power, light bus loading**
- **Functional similar to the 'F240 and 'F241**
- **Provides ideal interface and increases fan-out of MOS Microprocessors**
- **Efficient pinout to facilitate PC board layout**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

DESCRIPTION

The 74F540 and 74F541 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The devices feature input and outputs on opposite sides of the package to facilitate printed circuit board layout.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F540	3.5ns	58mA
74F541	5.5ns	55mA

ORDERING INFORMATION

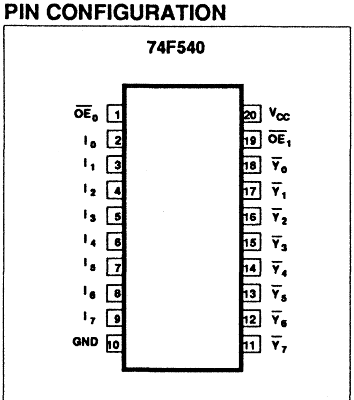
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F540N, N74F541N
20-Pin Plastic SOL	N74F540D, N74F541D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

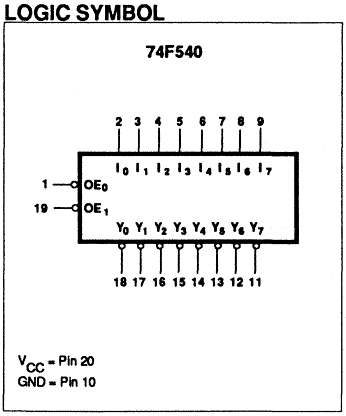
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0 - I_7	Data inputs	1.0/0.033	20µA/20µA
$\overline{OE}_0$, $\overline{OE}_1$	3-state output enable inputs (active Low)	1.0/0.033	20µA/20µA
Y_0 - Y_7	Data outputs ('F541)	750/106.7	15mA/64mA
$\overline{Y}_0$ - $\overline{Y}_7$	Data outputs ('F540)	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

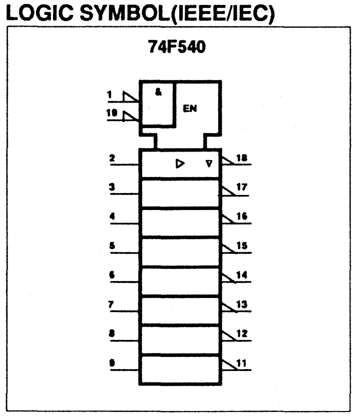
PIN CONFIGURATION



LOGIC SYMBOL



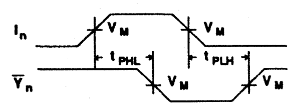
LOGIC SYMBOL(IEEE/IEC)



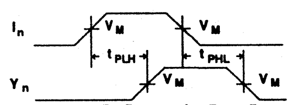
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Typ	Max	$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	74F540	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	74F540	Waveform 3 Waveform 4	2.0 4.0	3.5 7.5	6.5 9.5	2.0 4.0	7.0 10.0	ns
t_{PZH} t_{PZL}	Output Disable time from High or Low level	74F540	Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	74F541	Waveform 2	2.5 3.5	5.0 6.0	6.5 7.0	2.5 3.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	74F541	Waveform 6 Waveform 7	3.0 3.0	5.5 6.5	7.0 8.5	3.0 3.0	7.5 9.5	ns
t_{PZH} t_{PZL}	Output Disable time from High or Low level	74F541	Waveform 6 Waveform 7	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns

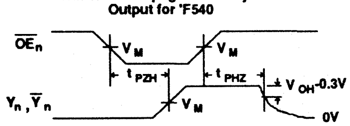
AC WAVEFORMS



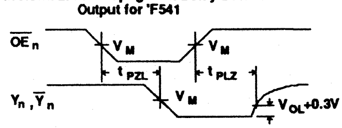
Waveform 1. For Propagation Delay Data to Output for 'F540



Waveform 2. For Propagation Delay Data to Output for 'F541



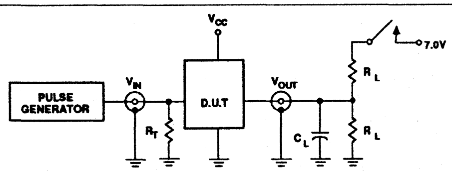
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



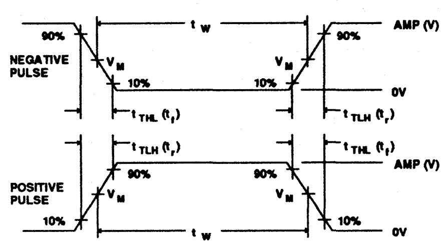
Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0874
ECN No.	99525
Date of issue	May 2, 1990
Status	Product Specification
FAST Products	

FAST 74F543, 74F544 Transceivers

74F543 Octal Registered Transceiver, Non-Inverting (3-State)
74F544 Octal Registered Transceiver, Inverting (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F543	6.0ns	80mA
74F544	6.5ns	95mA

FEATURES

- **Combines 74F245 and 74F373 type functions in one chip**
- **8-bit octal transceiver with D-type latch**
- **'F543 Non-Inverting**
  'F544 Inverting
- **Back-to-back registers for storage**
- **Separate controls for data flow in each direction**
- **A outputs sink 24mA and source 3mA**
- **B outputs sink 64mA and source 15mA**
- **300 mil wide 24-pin Slim DIP package**
- **3-state outputs for bus-orientated applications**

DESCRIPTION

The 74F543 and 74F544 Octal Registered Transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{\text{LEAB}}$, $\overline{\text{LEBA}}$) and Output Enable ($\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. While the 'F543 has non-inverting data path, the 'F544 inverts data in both directions. The A outputs are guaranteed to sink 24mA while the B outputs are rated for 64mA.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F543N, N74F544N
24-Pin Plastic SOL	N74F543D, N74F544D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F543 'F544	A_0 - A_7	Port A, 3-state inputs	3.5/1.0	70µA/0.6mA
	B_0 - B_7	Port B, 3-state inputs	3.5/1.0	70µA/0.6mA
	$\overline{\text{OEAB}}$	A-to-B Output Enable input (Active Low)	1.0/1.0	20µA/0.6mA
	$\overline{\text{OEBA}}$	B-to-A Output Enable input (Active Low)	1.0/1.0	20µA/0.6mA
	$\overline{\text{EAB}}$	A-to-B Enable input (Active Low)	1.0/2.0	20µA/1.2mA
	$\overline{\text{EBA}}$	B-to-A Enable input (Active Low)	1.0/2.0	20µA/1.2mA
	$\overline{\text{LEAB}}$	A-to-B Latch Enable input (Active Low)	1.0/1.0	20µA/0.6mA
	$\overline{\text{LEBA}}$	B-to-A Latch Enable input (Active Low)	1.0/1.0	20µA/0.6mA
'F543	A_0 - A_7	Port A, 3-state outputs	150/40	3.0mA/24mA
	B_0 - B_7	Port B, 3-state outputs	750/106.7	15mA/64mA
'F544	$\overline{A}_0$ - $\overline{A}_7$	Port $\overline{A}$, 3-state outputs	150/40	3.0mA/24mA
	$\overline{B}_0$ - $\overline{B}_7$	Port $\overline{B}$, 3-state outputs	750/106.7	15mA/64mA

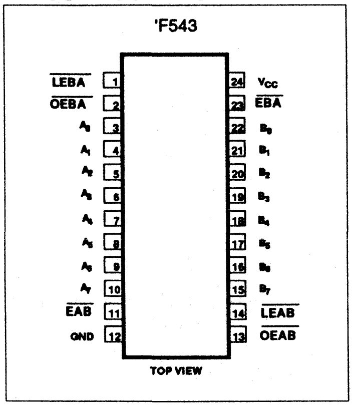
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

FUNCTIONAL DESCRIPTION

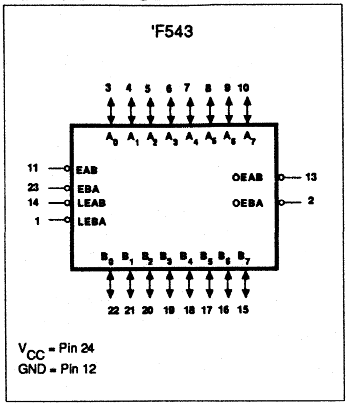
The 'F543 and 'F544 contain two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{\text{EAB}}$) input must be Low in order to enter data from A_0-A_7 or take data from B_0-B_7, as indicated in the Function Table. With $\overline{\text{EAB}}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{\text{LEAB}}$) input makes the A-to-B latches transparent; a subsequent Low-to High transition of the $\overline{\text{LEAB}}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{\text{EAB}}$ and $\overline{\text{OEAB}}$ both Low, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{\text{EBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

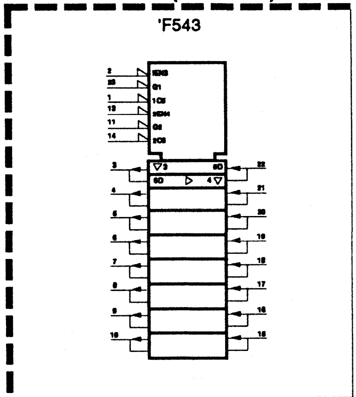
PIN CONFIGURATION



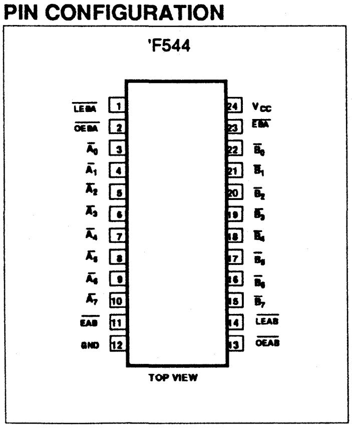
LOGIC SYMBOL



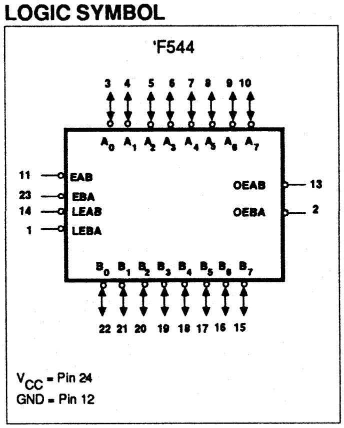
LOGIC SYMBOL(IEEE/IEC)



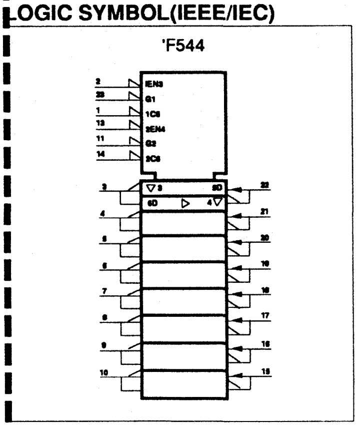
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



FUNCTION TABLE for 'F543 and 'F544

INPUTS				OUTPUTS		STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	DATA	'F543	'F544	
H	X	X	X	Z	Z	Disabled
X	H	X	X	Z	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	L H	Latch + Display
L L	L L	L L	H L	H L	L H	Transparent
L	L	H	X	NC	NC	Hold

H= High voltage level
L= Low voltage level
h= High state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to -High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
↑ =Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
X=Don't care
NC=No change
Z =High impedance "off" state

Document No.	853-1098
ECN No.	98906
Date of issue	February 23, 1990
Status	Product Specification
FAST Products	

FAST 74F552 Transceiver

Octal Registered Transceiver With Parity and Flags (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F552	85MHz	120mA

FEATURES

- **8-Bit bidirectional I/O port with handshake**
- **Register status flag flip-flops**
- **Separate clock enable and output enable**
- **Parity generation and parity check**
- **B outputs and parity output sink 64mA**

DESCRIPTION

The 74F552 Octal Registered Transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock (CPR, CPS) and Clock Enable ($\overline{CER}$, $\overline{CES}$) inputs, as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the Output Enable returns to High after reading the output port. Each register has a separate Output Enable ($\overline{OEAS}$, $\overline{OEBR}$) for its 3-state buffer. The separate Clocks, Flags and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data is transferred from the A port to the B port, a parity bit is generated. On the other hand, when data is transferred from the B port to the A port, the parity of input data on B_0-B_7 is checked.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (600mil)	N74F552N
28-Pin Plastic SOL[1]	N74F552D

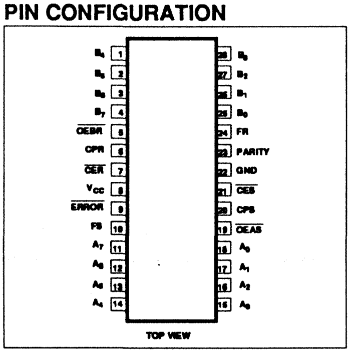
NOTE: Thermal mounting technique are recommended.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

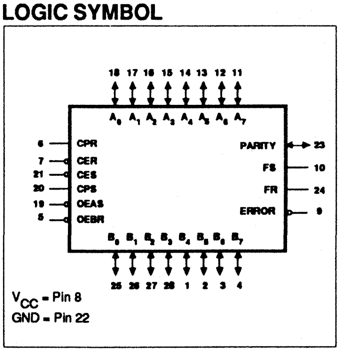
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A Data inputs	3.5/1.0	70µA/0.6mA
B_0 - B_7	B Data inputs	3.5/1.0	70µA/0.6mA
CPR	R registers clock input (active rising edge)	1.0/1.0	20µA/0.6mA
CPS	S registers clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{CER}$	R registers clock Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CES}$	S registers clock Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OEBR}$	A-to-B Output Enable input (active Low) and clear FS output (active Low)	1.0/2.0	20µA/1.2mA
$\overline{OEAS}$	B-to-A Output Enable input (active Low) and clear FR output (active Low)	1.0/2.0	20µA/1.2mA
PARITY	Parity bit transceiver input	3.5/1.0	70µA/0.6mA
	Parity bit transceiver output	750/106.7	15mA/64mA
$\overline{ERROR}$	Parity check output (active Low)	50/33.3	1.0mA/20mA
A_0 - A_7	A Data outputs	150/40	3.0mA/24mA
B_0 - B_7	B Data outputs	750/106.7	15mA/64mA
FR	A-to-B Status Flag output (active High)	50/33.3	1.0mA/20mA
FS	B-to-A Status Flag output (active High)	50/33.3	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

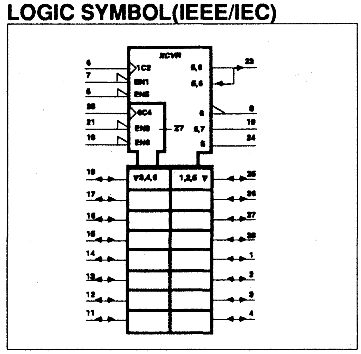
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Document No.	853-0166
ECN No.	98169
Date of issue	November 27, 1989
Status	Product Specification
FAST Products	

FAST 74F563, 74F564

Latch/Flip-Flop

74F563 Octal Transparent Latch (3-State)
74F564 Octal D Flip-Flop (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F563	5.0ns	40mA

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F564	180MHz	50mA

FEATURES

- **74F563 is broadside pinout version of 74F533**
- **74F564 is broadside pinout version of 74F534**
- **Inputs and Outputs on opposite side of package allow easy interface to Microprocessors**
- **Useful as an Input or Output port for Microprocessors**
- **3-State Outputs for Bus interfacing**
- **Common Output Enable**
- **74F573 and 74F574 are non-inverting versions of 74F563 and 74F564 respectively**
- **These are High-Speed replacements for N8TS807 and N8TS808**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F563N, N74F564N
20-Pin Plastic SOL	N74F563D, N74F564D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.6mA
E ('F563)	Latch Enable input (active High)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP ('F564)	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{Q}_0$ - $\overline{Q}_7$	3-State outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F563 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.
The 74F563 is functionally identical to the 74F533 but has a broadside pinout configuration to facilitate PC board layout and allows easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F564 is functionally identical to the 74F534 but has a broadside pinout configuration to facilitate PC board layout and allows easy interface with microprocessors.

It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's $\overline{Q}$ output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the register operation. When $\overline{OE}$ is Low, data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F563	Waveform 2	4.0 2.5	5.5 4.0	8.5 6.5	3.5 2.0	9.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}_n$	74F563	Waveform 1	5.0 3.0	6.5 5.0	9.5 7.0	4.5 3.0	10.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	74F563	Waveform 4 Waveform 5	2.5 4.0	4.5 6.0	7.5 8.0	2.5 3.5	8.5 8,5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	74F563	Waveform 4 Waveform 5	1.5 1.5	3.0 3.0	6.0 5.5	1.0 1.0	7.0 6.0	ns
f_{MAX}	Maximum Clock frequency	74F564	Waveform 1	160	180		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$	74F564	Waveform 1	3.5 3.5	5.0 5.0	8.0 8.0	3.0 3.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	74F564	Waveform 4 Waveform 5	2.5 4.0	4.5 5.5	7.5 8.0	2.0 3.5	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	74F564	Waveform 4 Waveform 5	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to E	74F563	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E	74F563	Waveform 3	3.0 2.5			3.0 2.5		ns
$t_w(H)$	E Pulse width, High	74F563	Waveform 1	3.5			3.5		ns
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	74F564	Waveform 3	2.0 2.0			2.0 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP	74F564	Waveform 3	1.0 1.0			1.5 1.5		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	74F564	Waveform 1	3.5 3.5			3.5 3.5		ns

Document No.	853-0083
ECN No.	97897
Date of issue	October 16, 1989
Status	Product Specification
FAST Products	

FAST 74F573, 74F574
Latch/Flip-Flop

74F573 Octal Transparent Latch (3-State)
74F574 Octal D Flip-Flop (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F573	5.0ns	35mA

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F574	180MHz	50mA

FEATURES
- **74F573 is broadside pinout version of 74F373**
- **74F574 is broadside pinout version of 74F374**
- **Inputs and Outputs on opposite side of package allow easy interface to Microprocessors**
- **Useful as an Input or Output port for Microprocessors**
- **3-State Outputs for Bus Interfacing**
- **Common Output Enable**
- **74F563 and 74F564 are inverting version of 74F573 and 74F574 respectively**
- **3-State Outputs glitch free during power-up and power-down**
- **These are High-Speed replacements for N8TS805 and N8TS806**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F573N, N74F574N
20-Pin Plastic SOL	N74F573D, N74F574D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.6mA
E ('F573)	Latch enable input (active falling edge)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
CP ('F574)	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	3-State outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F573 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.
The 74F573 is functionally identical to the 74F373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F574 is functionally identical to the 74F374 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F573	V_{CC} = MAX			30	40	mA
		I_{CCL}					35	50	mA
		I_{CCZ}					40	60	mA
		I_{CCH}	74F574	V_{CC} = MAX			45	65	mA
		I_{CCL}					50	70	mA
		I_{CCZ}					55	85	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F573	Waveform 2	3.0 1.0	5.5 3.5	8.0 6.0	2.5 1.0	9.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n	74F573	Waveform 1	4.5 3.0	8.5 5.0	11.5 7.0	4.0 2.5	12.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	74F573	Waveform 5 Waveform 6	2.5 2.5	5.5 5.5	9.5 8.0	2.0 2.0	10.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	74F573	Waveform 5 Waveform 6	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	6.5 5.5	ns
f_{MAX}	Maximum Clock frequency	74F574	Waveform 1	160	180		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	74F574	Waveform 1	3.5 3.5	5.0 5.0	7.5 7.5	3.0 3.0	8.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	74F574	Waveform 5 Waveform 6	2.5 3.0	4.5 5.0	7.5 8.0	2.0 3.0	7.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	74F574	Waveform 5 Waveform 6	1.0 1.0	3.0 2.5	5.5 5.5	1.0 1.0	6.0 6.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to E	74F573	Waveform 4	0.0 1.5			0.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E	74F573	Waveform 4	2.5 4.0			2.5 4.0		ns
$t_w(H)$	E Pulse width, High	74F573	Waveform 1	3.0			3.5		ns
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	74F574	Waveform 3	2.5 2.5			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP	74F574	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	74F574	Waveform 1	3.0 3.5			3.0 4.0		ns

Document No.	853-0377
ECN No.	99600
Date of issue	May 15, 1990
Status	Product Specification
FAST Products	

FAST 74F579 Counter

8-Bit Bidirectional Binary Counter (3-state)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F579	115MHz	100mA

FEATURES

- **Fully synchronous operation**
- **Multiplexed 3-state I/O ports for bus oriented applications**
- **Built in cascading carry capability**
- **U/$\overline{D}$ pin to control direction of counting**
- **Separate pins for Master Reset and Synchronous operation**
- **Center power pins to reduce effects of package inductance**
- **Count frequency 115MHz typ**
- **Supply current 100mA typ**
- **See 'F269 for 24 pin separate I/O port version**
- **See 'F779 for 16 pin version**

DESCRIPTION

The 74F579 is a fully synchronous 8-stage Up/Down Counter with multiplexed 3-state I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock. $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

ORDERING INFORMATION

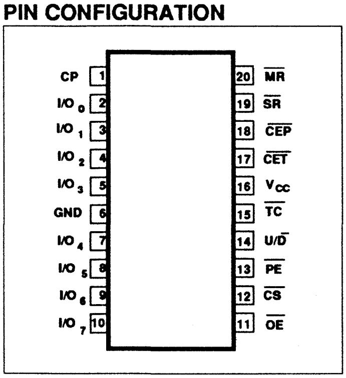
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic Dip	N74F579N
20-Pin Plastic SOL	N74F579D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

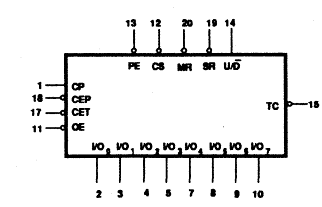
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Data inputs	3.5/1.0	70µA/0.6mA
	Data outputs	150/40	3.0mA/24mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable Parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

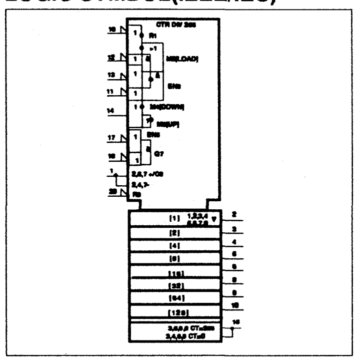


LOGIC SYMBOL

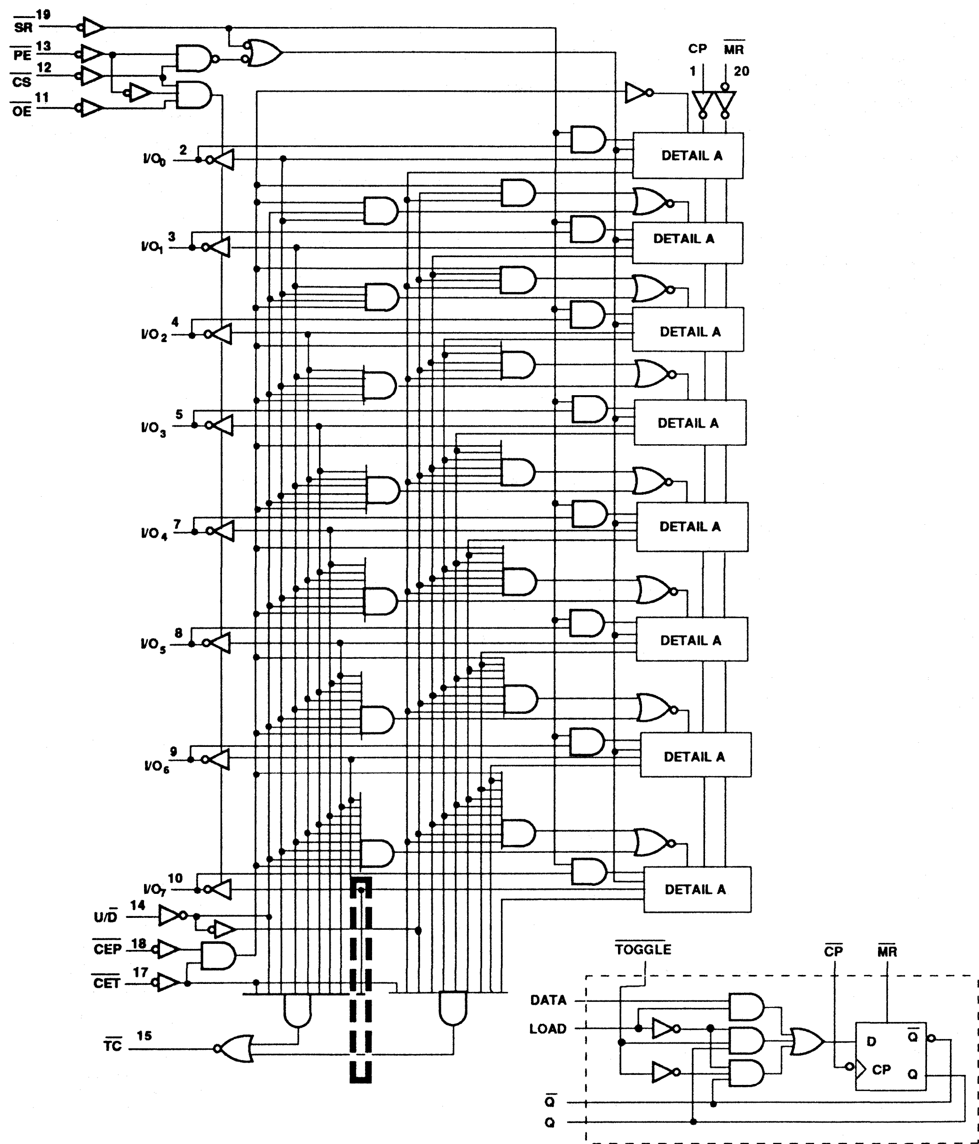


V_{CC} = Pin 16
GND = Pin 6

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



DETAIL A

V_{CC} =pin16
GND=pin 6

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	5.0 5.0	7.5 7.5	10.5 10.5	5.0 5.0	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 5.5	7.5 7.5	10.0 10.0	5.0 5.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $U/\overline{D}$ to $\overline{TC}$	Waveform 4	3.5 4.5	5.5 6.5	8.0 8.0	3.5 4.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 3	3.5 3.5	5.5 6.0	7.0 8.0	3.5 3.5	8.5 8.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 2	5.0	7.0	9.0	5.0	10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{CS}$ to I/O_n	Waveform 6 Waveform 7	4.0 5.5	5.0 7.0	8.5 10.5	3.5 5.0	10.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{CS}$ to I/O_n	Waveform 6 Waveform 7	3.0 5.0	5.0 7.5	7.5 9.5	3.0 4.5	9.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	3.0 5.0	4.5 6.5	8.0 10.0	3.0 4.5	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	3.0 2.5	4.0 4.0	7.5 7.5	3.0 2.0	9.0 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	2.5 4.5	4.0 5.5	7.0 9.0	2.5 4.0	8.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	1.0 2.0	2.5 4.0	4.0 7.0	1.0 2.0	5.5 8.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 5	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $U/\overline{D}$ to CP	Waveform 5	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $U/\overline{D}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	9.5 9.5			10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	5.0 9.0			5.5 10.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.5 4.5			4.5 4.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	3.0			3.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

Document No.	853-1247
ECN No.	99495
Date of issue	April 27, 1990
Status	Product Specification
FAST Products	

FAST 74F582
4-Bit BCD Arithmetic Logic Unit

FEATURES
- Performs four BCD functions
- $\overline{P}$ and $\overline{G}$ outputs for high speed expansion
- Add/Subtract delay 28ns max
  Look ahead delay 22.5ns max
- Supply current 85mA max
- 24 pin 300 mil Slim Dip package

DESCRIPTION
The 74F582 Binary Coded Decimal (BCD) Arithmetic Logic Unit (ALU) is a 24 pin expandable unit that performs addition, subtraction, comparison of two numbers and binary to BCD conversion.

The 'F582 input and output logic includes a Carry/$\overline{\text{Borrow}}$ which is generated internally in the look-ahead mode, allowing BCD to computed directly.

CASCADING FEATURE IS DELETED

When $\overline{A}$/S is Low, BCD addition is performed (A+B+C/$\overline{B}$=F). If an input is greater than 9 binary to BCD conversion results at the output.

When $\overline{A}$/S is High, subtraction is performed. If the C/$\overline{B}$ is Low, then the subtraction is accomplished by internally computing the nine's complement addition of the two BCD numbers(A-B-1=F). When C/$\overline{B}$ is High, the difference of the two numbers is figured as A-F=F. If A is greater than or equal to B, the BCD difference appears at the output F in its true form. If A is less than B and C/$\overline{B}$ is Low, the 9s complement of the true form appears at the output F. As long as A is less than B, an active Low borrow is also generated. The 'F582 also performs binary to BCD conversion. For inputs from 10 to 15, binary to BCD conversion occurs by grounding one set of inputs, A_n or B_n, and applying the binary number to the other set of inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F582	12.0 ns	55mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F582N
24-Pin Plastic SOL	N74F582D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_3	A operand inputs	1.0/2.0	20µA/1.2mA
B_0	B operand input	1.0/1.0	20µA/0.6mA
B_1	B operand input	1.0/4.0	20µA/2.4mA
B_2	B operand input	1.0/3.0	20µA/1.8mA
B_3	B operand input	1.0/2.0	20µA/1.2mA
$\overline{A}$/S	Add/Subtract input	1.0/3.0	20µA/1.8mA
C/$\overline{B}$	Carry/Borrow input	1.0/1.0	20µA/0.6mA
C/$\overline{B}_{n+4}$	Carry/Borrow output	50/33	1.0mA/20mA
$\overline{P}$	Carry Propagate output	50/33	1.0mA/20mA
$\overline{G}$	Carry Generator output	50/33	1.0mA/20mA
A=B	Comparator output	OC/33	OC/20mA
F_0-F_3	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

Document No.	853-1096
ECN No.	99392
Date of issue	April 18, 1990
Status	Product Specification
FAST Products	

FAST 74F595
Shift Register

8-Bit Shift Register with Output Latches (3-state)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F595	130MHz	65mA

FEATURES
- **Low noise, no switching feedthru current**
- **Controlled output edge rates**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **8-bit serial-in, parallel-out shift register with storage**
- **3-state outputs**
- **Shift register has direct clear**
- **Guaranteed shift frequency-DC to 100MHz**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F595N
16-Pin Plastic SO	N74F595D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_S	Serial data input	1.0/0.033	20μA/20μA
SHCP	Shift register clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
STCP	Storage register clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
$\overline{SHR}$	Shift register reset input (active Low)	1.0/0.033	20μA/20μA
$\overline{OE}$	Output enable input (active Low)	1.0/0.033	20μA/20μA
Q_S	Serial expansion output	50/33	1.0mA/20mA
Q_0 - Q_7	Data outputs	150/40	3.0mA/24mA

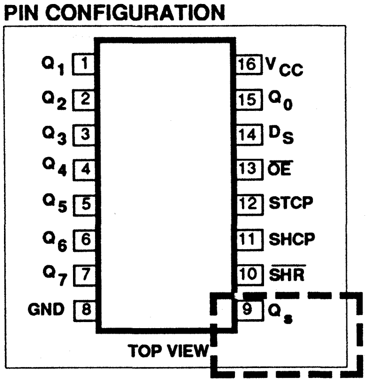
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

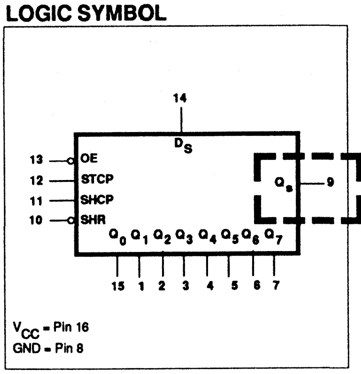
The 74F595 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct overriding clear, serial input and serial output pins for cascading. Both the shift register and storage register clocks are positive edge-triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

This device uses patented circuitry to control system noise and internal ground bounce. This is done by eliminating switching feedthru current and controlling both Low-to-High and High-to-Low slew rates.

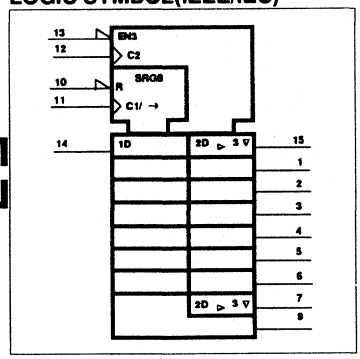
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	SHCP to Q_S	Waveform 1	115	135		90		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_S		Waveform 1	6.0 2.5	8.0 4.5	10.5 7.5	5.0 2.5	12.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q_0 - Q_7		Waveform 1	5.5 3.0	8.0 5.0	10.0 8.0	4.5 3.0	13.0 8.5	ns
t_{PHL}	Propagation delay $\overline{SHR}$ to Q_S		Waveform 2	3.5	5.5	8.0	3.0	8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_0 - Q_7		Waveform 5 Waveform 6	3.5 3.0	5.5 5.5	9.0 8.5	2.5 2.5	10.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ or Q_0 - Q_7		Waveform 5 Waveform 6	2.0 4.0	4.0 6.0	7.0 9.0	1.5 3.0	8.5 10.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_S to SHCP	Waveform 3	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_S to SHCP	Waveform 3	0 0			0 0		ns
$t_s(L)$	Setup time, Low $\overline{SHR}$ to STCP	Waveform 3	4.5			5.0		ns
$t_s(H)$	Setup time, High SHCP to STCP	Waveform 4	4.5			5.0		ns
$t_w(H)$ $t_w(L)$	SHCP Pulse width, High or Low	Waveform 1	3.5 4.0			4.0 4.0		ns
$t_w(H)$ $t_w(L)$	STCP Pulse width, High or Low	Waveform 1	4.0 3.0			4.0 3.5		ns
$t_w(L)$	$\overline{SHR}$ Pulse width, Low	Waveform 2	3.0			3.0		ns
t_{REC}	Recovery time, $\overline{SHR}$ to SHCP	Waveform 2	3.0			3.0		ns

Document No.	853-
ECN No.	
Date of issue	February 1, 1990
Status	Preliminary Specification
FAST Products	

FAST 74F597, 74F598

Shift Registers

74F597 8-Bit Shift Register with Input Storage Registers
74F598 8-Bit Shift Register with Input Storage Registers (3-State)

FEATURES

- **High impedance NPN base input for reduced loading (20μA in High and Low states)**
- **8-bit Parallel storage register**
- **Shift register has asynchronous direct overriding load and reset**
- **Guaranteed shift frequency DC to 120MHz**
- **Parallel 3-State I/O, Storage register inputs**
- **Shift register outputs-'F598**

DESCRIPTION

The 74F597 consists of an 8-bit storage register feeding a parallel-in/serial-in, serial out 8-bit shift register. The storage register and shift register have separate positive edge triggered clocks. The shift register also has asynchronous direct load (from storage) and reset inputs.

The 74F598 consists of an 8-bit storage register feeding a parallel/serial-in, parallel/serial out 8-bit shift register. Both the storage register and shift register have positive edge triggered clocks. The shift register also has asynchronous direct load (from storage) and reset inputs. The 'F598 has 3-state I/O ports that provide parallel shift register outputs and also has multiplexed serial data input.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F597	120MHz	75mA
74F598	120MHz	75mA

ORDERING INFORMATION

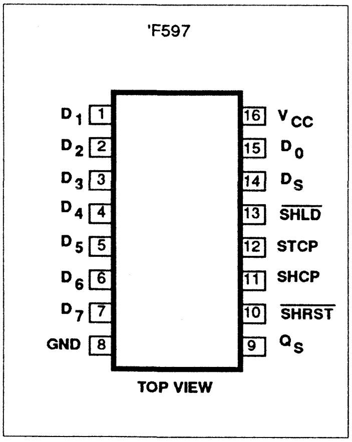
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F597N
20-Pin Plastic DIP	N74F598N
16-Pin Plastic SO	N74F597D
20-Pin Plastic SOL	N74F598D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

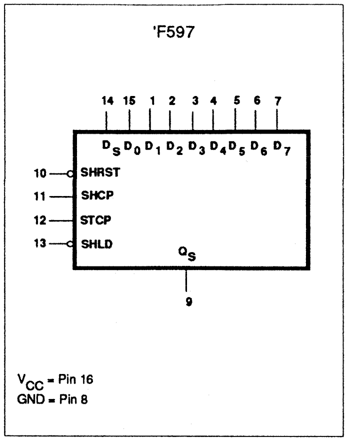
	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
	D_S	Serial data input	1.0/0.033	20μA/20μA
	D_0-D_7	Parallel data inputs	1.0/0.033	20μA/20μA
	SHCP	Shift register clock pulse input	1.0/0.033	20μA/20μA
'F597	STCP	Storage register clock pulse input	1.0/0.033	20μA/20μA
	$\overline{SHLD}$	Shift register load input (active Low)	1.0/0.033	20μA/20μA
	$\overline{SHRST}$	Shift register reset input (active Low)	1.0/0.033	20μA/20μA
	Q_S	Serial data output	50/33	1.0mA/20mA
	I/O_n	Parallel data inputs	1.0/0.033	20μA/20μA
	D_{S0}, D_{S1}	Serial data inputs	1.0/0.033	20μA/20μA
	SHCP	Shift register clock pulse input	1.0/0.033	20μA/20μA
	$\overline{STCP}$	Storage register clock pulse input	1.0/0.033	20μA/20μA
'F598	$\overline{SHCPEN}$	Shift register clock pulse enable input	1.0/0.033	20μA/20μA
	$\overline{SHLD}$	Shift register load input (active Low)	1.0/0.033	20μA/20μA
	$\overline{SHRST}$	Shift register reset input (active Low)	1.0/0.033	20μA/20μA
	S	Serial data selector input	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output Enable input	1.0/0.033	20μA/20μA
	Q_S	Serial data output	50/33	1.0mA/20mA
	I/O_n	Parallel data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

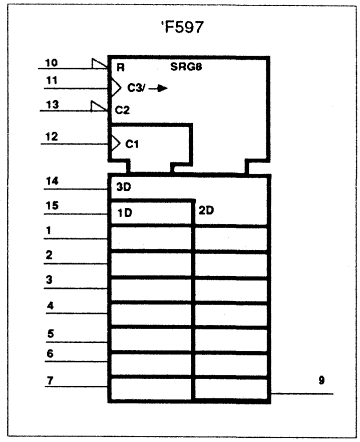
PIN CONFIGURATION



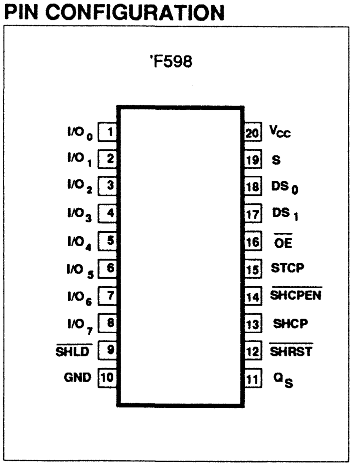
LOGIC SYMBOL



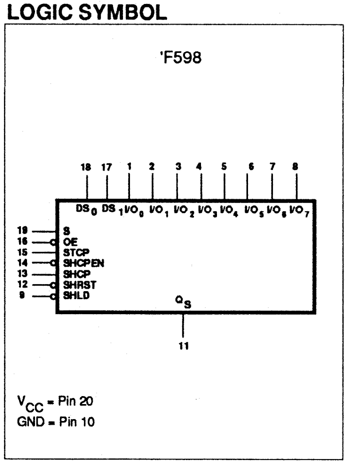
LOGIC SYMBOL(IEEE/IEC)



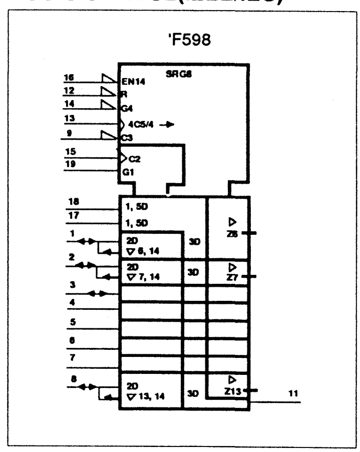
PIN CONFIGURATION



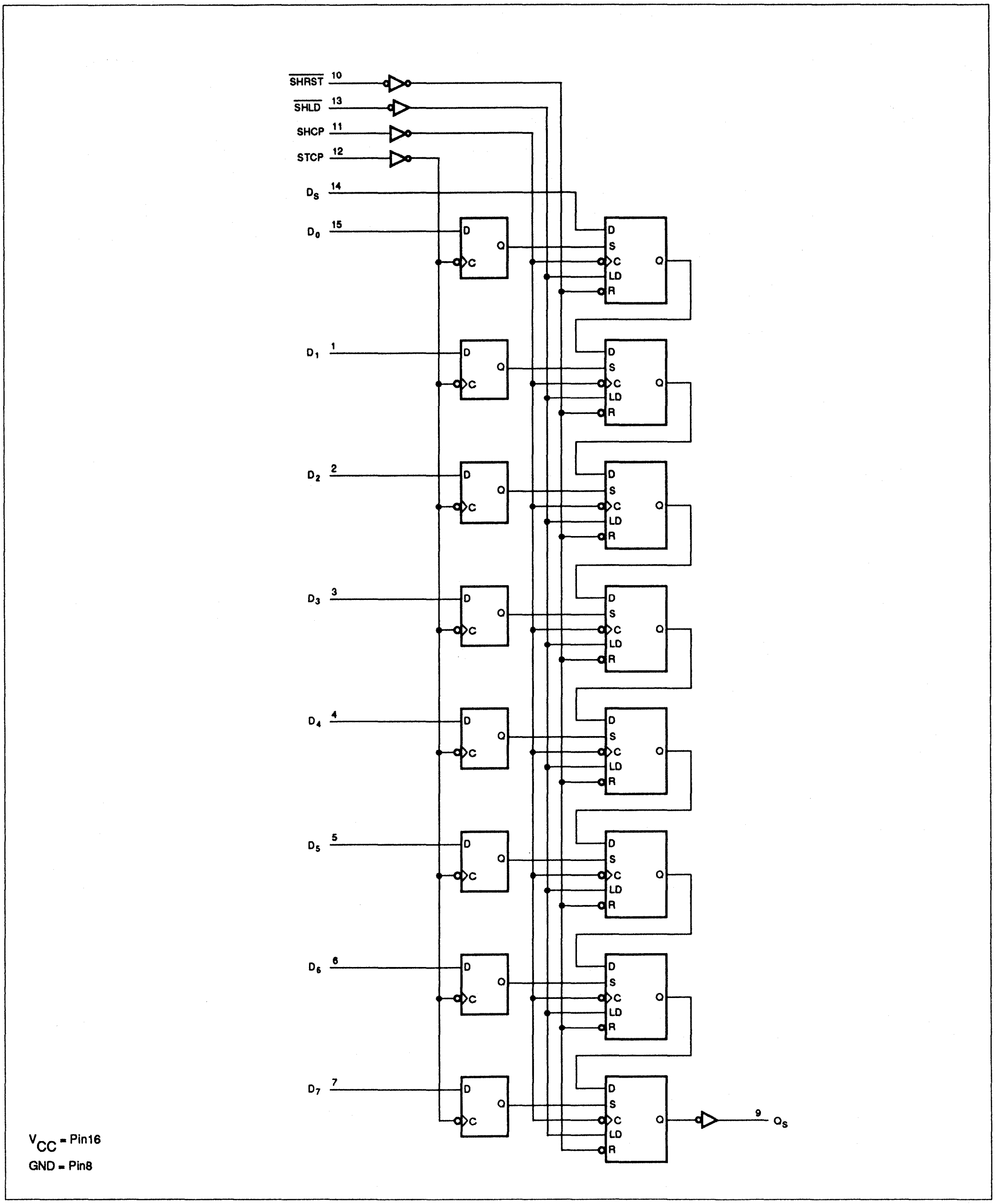
LOGIC SYMBOL



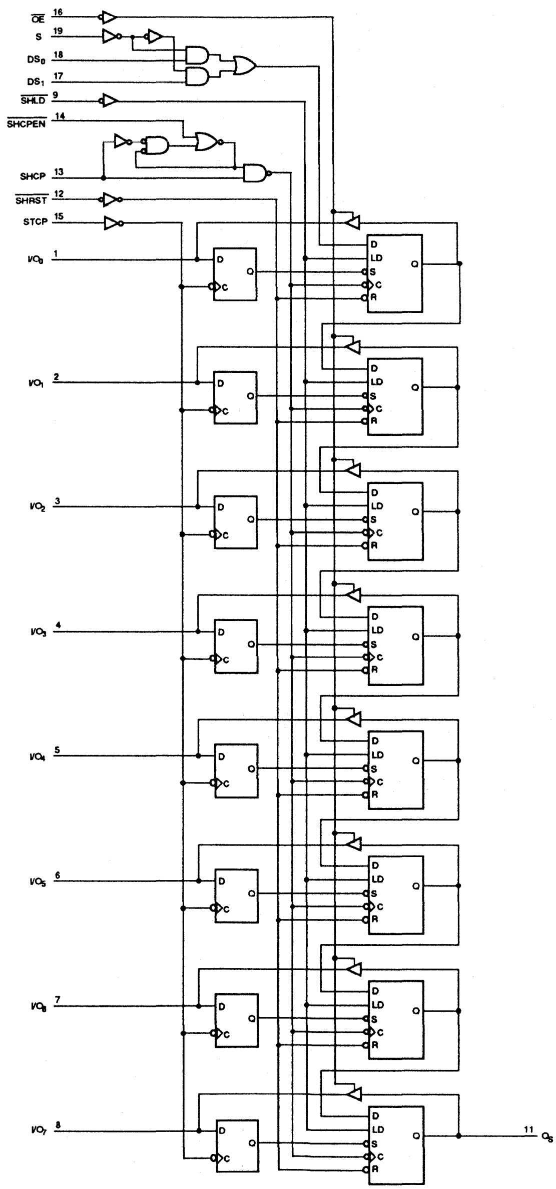
LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM for 'F597



LOGIC DIAGRAM FOR 'F598



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS				OPERATING MODES
STCP	SHCP	$\overline{SHLD}$	$\overline{SHRST}$	
↑	X	X	X	data loaded to storage registers
↑	X	L	H	data loaded from inputs to shift register
$\not\uparrow$	X	L	H	data transferred from storage registers to shift registers
X	X	L	L	Invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked, $Q_n = Q_{n-1}$, $Q_0 = Q_S$

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low to High clock transition
$\not\uparrow$ = Not Low to High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	Q_S	40	mA
		I/O_0- I/O_7	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_S			-1	mA
		I/O_0- I/O_7			-3	mA
I_{OL}	Low-level output current	Q_S			20	mA
		I/O_0- I/O_7			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	Q_S	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MI	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		I/O_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
$I_{OZH}+I_{IH}$	Off-state output current, High-level voltage applied	I/O_n only	V_{CC} = MAX, V_O= 2.7V					70	µA
$I_{OZL}+I_{IL}$	Off-state output current, Low-level voltage applied	I/O_n only	V_{CC} = MAX, V_O= 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	'F597 I_{CCH}	V_{CC} = MAX				45	70	mA
		'F597 I_{CCL}					48	75	mA
		'F597 I_{CCZ}					75	90	mA
		'F598 I_{CCH}					78	95	mA
		'F598 I_{CCL}					85	100	mA
		'F598 I_{CCH}							

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 'F597

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		80		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_S	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	9.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to Q_S	Waveform 1	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q_S	Waveform 1	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PHL}	Propagation delay $\overline{SHRST}$ to Q_S	Waveform 3	4.0	8.0	10.0	4.0	11.0	ns

AC SETUP REQUIREMENTS for 'F597

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to STCP	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to STCP	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_S to SHCP	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_S to SHCP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low STCP to $\overline{SHLD}$	Waveform 4	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low STCP to $\overline{SHLD}$	Waveform 4	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	SHCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(H)$ $t_w(L)$	STCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{SHRST}$ pulse width, Low	Waveform 1	4.0			4.0		ns
$t_w(L)$	$\overline{SHLD}$ pulse width, Low	Waveform 1	4.0			4.0		ns
t_{REC}	Recovery time, $\overline{SHRST}$ to SHCP	Waveform 2	6.0			7.0		ns
t_{REC}	Recovery time, $\overline{SHLD}$ to SHCP	Waveform 2	6.0			7.0		ns

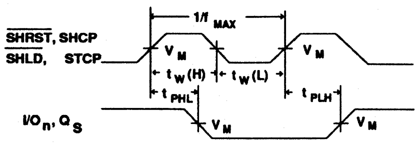
AC ELECTRICAL CHARACTERISTICS for 'F598

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		80		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_S	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q_S ($\overline{SHLD}$ =Low)	Waveform 1	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to Q_S	Waveform 1	4.0 4.0	7.5 8.0	9.0 9.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay SHCP to I/O_n	Waveform 1	4.0 4.0	7.5 8.0	9.0 9.0	4.0 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHRST}$ to Q_S	Waveform 1	4.0 4.0	7.5 8.0	9.0 9.0	4.0 4.0	10.0 10.0	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to I/O_S	Waveform 2	4.0	8.0	10.0	4.0	11.0	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to Q_S	Waveform 2	4.0	8.0	10.0	4.0	11.5	ns
t_{PZH} t_{PHZ}	Output Enable time to High or Low	Waveform 5 Waveform 6	4.0 4.0	7.5 7.5	9.0 9.0	4.0 4.0	10.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low	Waveform 5 Waveform 6	3.0 3.0	6.0 6.0	8.0 8.0	3.0 3.0	9.0 9.0	ns

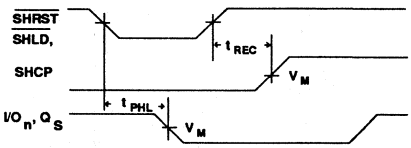
AC SETUP REQUIREMENTS for 'F598

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_{Sn} to SHCP	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_{Sn} to SHCP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low STCP to $\overline{SHLD}$	Waveform 4	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low STCP to $\overline{SHLD}$	Waveform 4	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SHCPEN}$ to SHCP	Waveform 3	6.0 6.0			4.0 5.0		ns
$t_w(H)$ $t_w(L)$	SHCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(H)$ $t_w(L)$	STCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{SHRST}$ pulse width, Low	Waveform 1	4.0			4.0		ns
$t_w(L)$	$\overline{SHLD}$ pulse width, Low	Waveform 1	4.0			4.0		ns
t_{REC}	Recovery time, $\overline{SHRST}$ to SHCP	Waveform 2	6.0			7.0		ns
t_{REC}	Recovery time, $\overline{SHLD}$ to SHCP	Waveform 2	6.0			7.0		ns

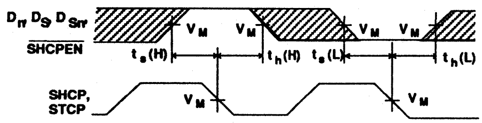
AC WAVEFORMS



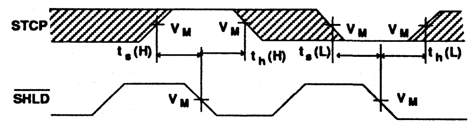
Waveform 1. Propagation Delay, Clock Inputs To Output, Clock Pulse Width, Maximum Clock Frequency, Shift Register Reset And Load Inputs To Serial Data Output



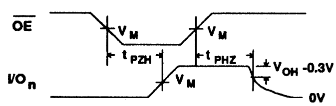
Waveform 2. Propagation Delay, Shift Register Reset And Load InputsTo Serial Data Output, Shift Register Reset And Load Inputs To Shift register Clock Pulse Input Recovery Time



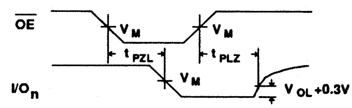
Waveform 3. Setup And Hold Times



Waveform 4. Setup And Hold Times



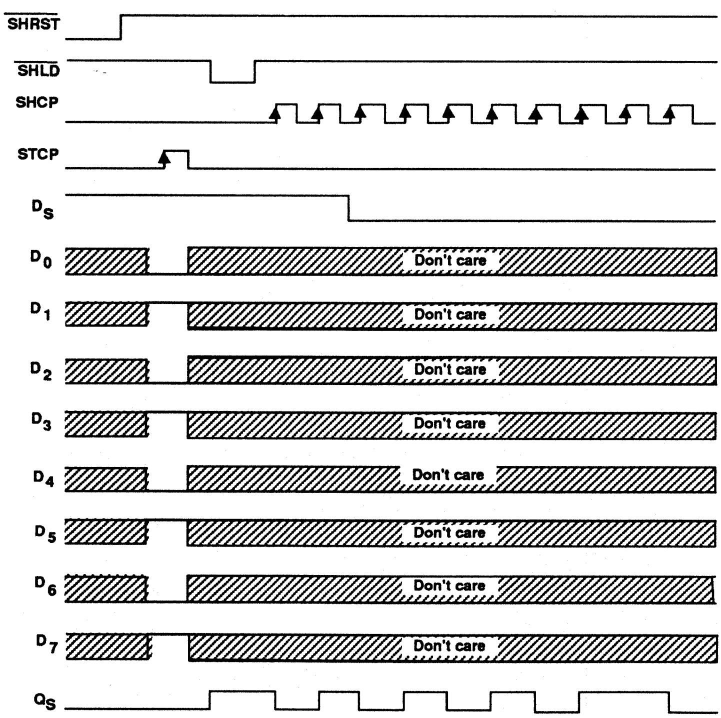
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



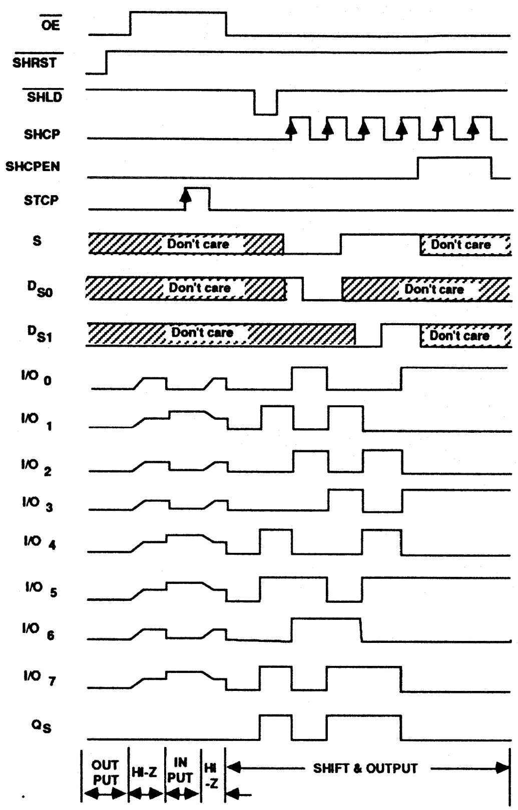
Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

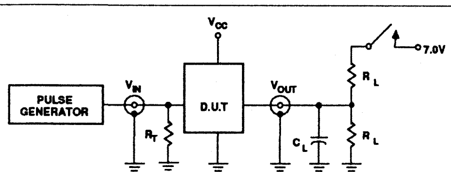
TYPICAL TIMING DIAGRAM for 74F597



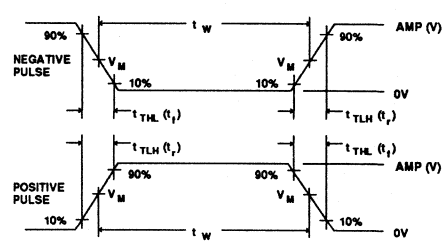
TYPICAL TIMING DIAGRAM for 74F598



TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0029
ECN No.	98991
Date of issue	March 1, 1990
Status	Product Specification
FAST Products	

FAST 74F604

Latch

Dual Octal Latch (3-State)

FEATURES

- **High impedance NPN base inputs for reduced loading (20µA in High and Low states)**
- **Stores 16-bit-wide Data inputs, multiplexed 8-bit outputs**
- **3-state outputs**
- **Power supply current 75mA typical**

DESCRIPTION

The 74F604 multiplexed latch is ideal for storing data from two input buses, A or B, and providing data from either the A or B latches to the output bus. Organized as 8-bit A and B latches, the latch outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT A/$\overline{B}$) input determines whether the A or B latch contents are multiplexed to the eight 3-state outputs. Data entered from the B inputs are selected when SELECT A/$\overline{B}$ is Low; data from the A inputs are selected when SELECT A/$\overline{B}$ is High. Data enters the latches when the Latch Enable ($\overline{LE}$) input is Low and is latched on the $\overline{LE}$ rising edge. The outputs are enabled when $\overline{LE}$ is High and disabled when $\overline{LE}$ is Low.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F604	7.5ns	75mA

ORDERING INFORMATION

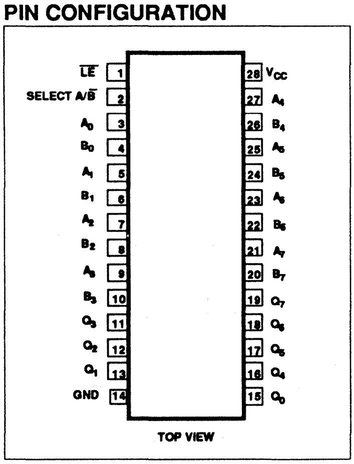
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F604N
28-Pin Plastic SOL	N74F604D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

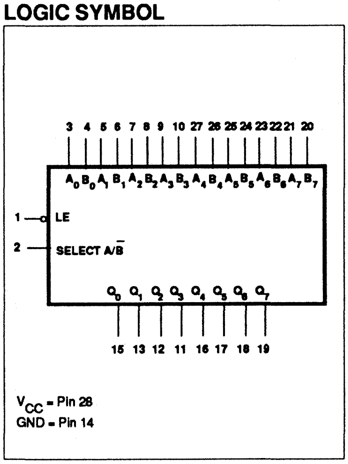
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7, B_0-B_7	Data inputs	1.0/0.033	20µA/20µA
SELECT A/$\overline{B}$	Select input	1.0/0.033	20µA/20µA
$\overline{LE}$	Latch Enable Input (active Low)	1.0/0.033	20µA/20µA
Q_0-Q_7	Data outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

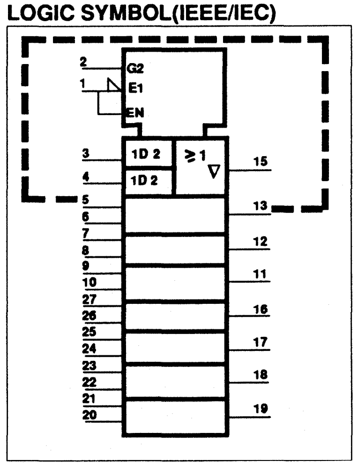
PIN CONFIGURATION



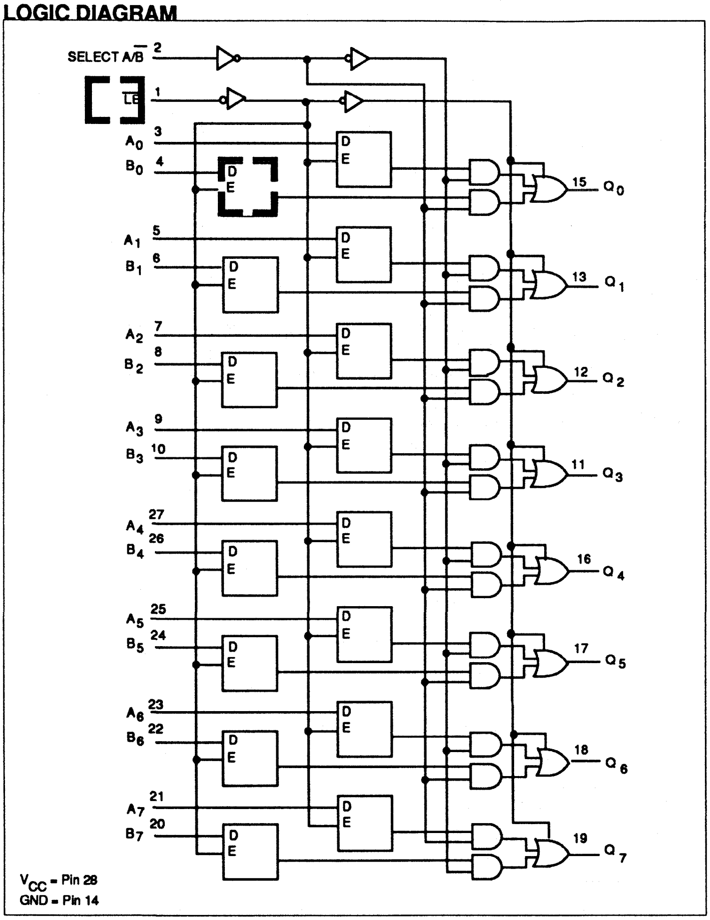
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
A_0-A_7	B_0-B_7	SELECT A/$\overline{B}$	$\overline{LE}$	Q_0-Q_7
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z
X	X	L	H	B latched data
X	X	H	H	A latched data

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High transition

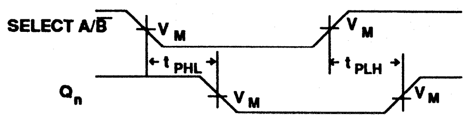
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (B latch)	Waveform 1	5.0 6.0	7.0 8.5	9.0 10.5	4.5 5.5	10.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (A latch)	Waveform 2	6.0 4.0	8.0 6.5	10.0 8.5	5.5 3.5	11.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	5.0 5.0	7.5 7.5	9.5 9.5	4.5 4.5	10.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 4 Waveform 5	5.0 5.0	7.0 7.0	9.5 9.5	4.5 4.5	11.0 11.0	ns

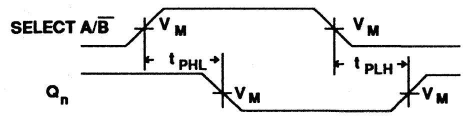
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n ,B_n to $\overline{LE}$	Waveform 3	1.0 2.0			2.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n ,B_n to $\overline{LE}$	Waveform 3	0 1.0			0 1.5		ns
$t_w(L)$	$\overline{LE}$ Pulse width, Low	Waveform 3	5.0			6.0		ns

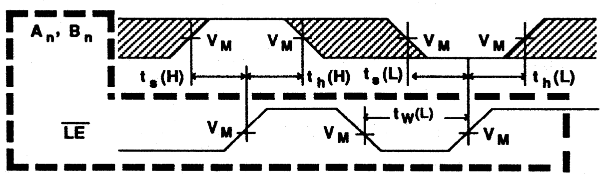
AC WAVEFORMS



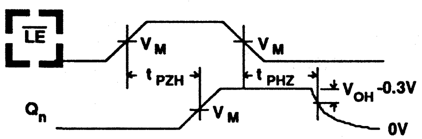
Waveform 1. Propagation Delay, SELECT A/$\overline{B}$ To Output (B latched data=Low. $\overline{LE}$=H)



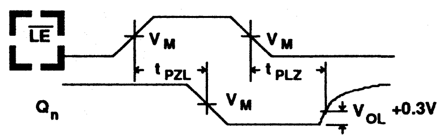
Waveform 2. Propagation Delay, SELECT A/$\overline{B}$ To Output (A latched data=Low. $\overline{LE}$=H)



Waveform 3. Data Setup And Hold Times ,Latch Enable pulse width



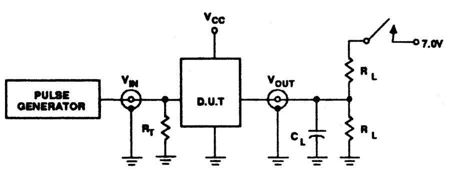
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

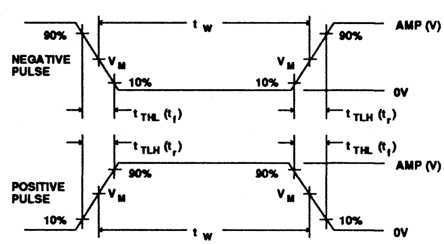
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0030
ECN No.	97679
Date of issue	September 20, 1989
Status	Product Specification
FAST Products	

FAST 74F605

Latch

Dual Octal Latch (Open Collector)

FEATURES

- **High impedance NPN base inputs for reduced loading (20µA in High and Low states)**
- **Stores 16-bit-wide Data inputs, multiplexed 8-bit outputs**
- **Open Collector outputs**
- **Propagation delay 10ns typical**
- **Power supply current 85mA typical**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F605	10.0ns	85mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V\pm10\%$; $T_A = 0°C$ to $+70°C$
28-Pin Plastic DIP	N74F605N
28-Pin Plastic SOL	N74F605D

DESCRIPTION

The 74F605 multiplexed latch is ideal for storing data from two input buses, A or B, and providing data from either the A or B latches to the ouput bus. Organized as 8-bit A and B latches, thelatch outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT $A/\overline{B}$) input determines whether the A or B latch contents are multiplexed to the eight Open Collector outputs. Data entered from the B inputs are selected when SELECT $A/\overline{B}$ is Low; data from the A inputs are selected when SELECT $A/\overline{B}$ is High. Data enters the latches when the Latch Enable ($\overline{LE}$) input is Low and is latched on the $\overline{LE}$ rising edge. The outputs are enabled when $\overline{LE}$ is High and disabled when $\overline{LE}$ is Low.

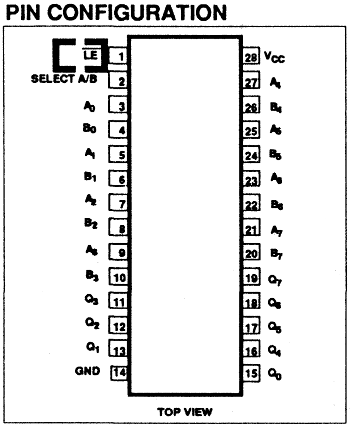
These functions are also well-suited for receiving 16-bit simultaneous data and transmitting it as two sequential 8-bit words.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

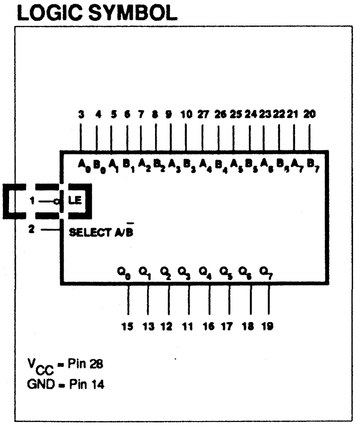
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7, B_0-B_7	Data inputs	1.0/0.033	20µA/20µA
SELECT $A/\overline{B}$	Select input	1.0/0.033	20µA/20µA
$\overline{LE}$	Latch Enable Input (active Low)	1.0/0.033	20µA/20µA
Q_0-Q_7	Data outputs	OC/40	OC/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC = Open Collector

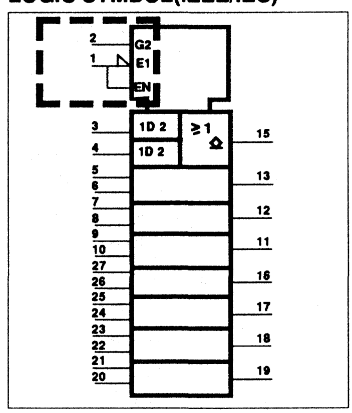
PIN CONFIGURATION



LOGIC SYMBOL



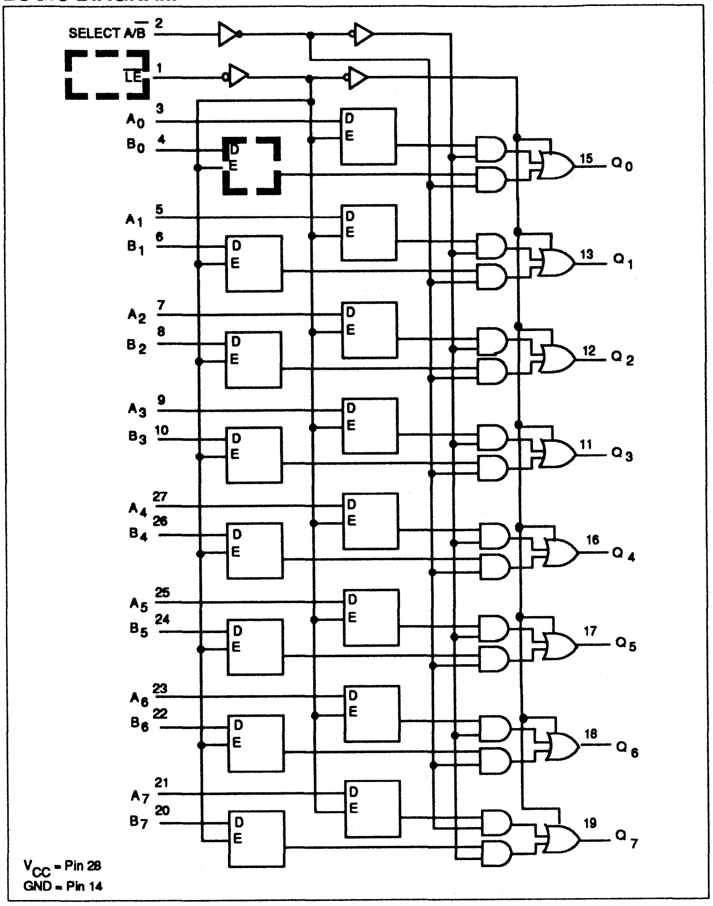
LOGIC SYMBOL(IEEE/IEC)



Latch

FAST 74F605

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
A_0-A_7	B_0-B_7	SELECT A/$\overline{B}$	$\overline{LE}$	Q_0-Q_7
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	OFF
X	X	L	H	B latched data
X	X	H	H	A latched data

H = High voltage level
L = Low voltage level
X = Don't care
OFF= Pulled up through resistor (open collector)
↑ =Low-to-High transition

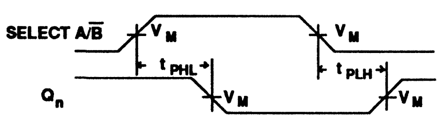
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (B latch)	Waveform 2	7.5 7.5	9.5 10.0	11.5 12.0	7.0 7.0	12.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (A latch)	Waveform 1	8.5 6.5	11.0 8.5	13.0 11.0	8.0 6.0	14.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to Q_n	Waveform 3	8.5 6.5	11.0 9.0	13.0 11.0	8.0 6.0	14.5 12.0	ns

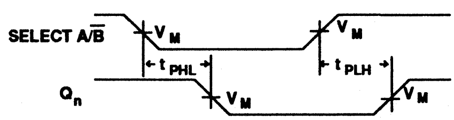
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n, B_n to $\overline{LE}$	Waveform 4	1.0 3.0			2.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n, B_n to $\overline{LE}$	Waveform 4	1.0 2.0			2.0 3.0		ns
$t_w(L)$	$\overline{LE}$ Pulse width, Low	Waveform 4	5.0			6.0		ns

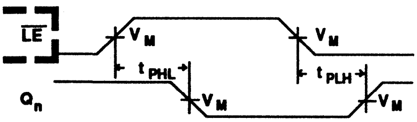
AC WAVEFORMS



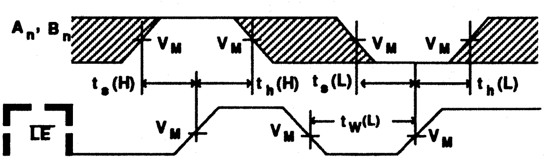
Waveform 1. Propagation Delay, SELECT A/$\overline{B}$ To Output (A latched data=Low. $\overline{LE}$=H)



Waveform 2. Propagation Delay, SELECT A/$\overline{B}$ To Output (B latched data=Low. $\overline{LE}$=H)



Waveform 3. Propagation Delay, Clock To Output (A latched data=Low. SELECT A/$\overline{B}$=H)



Waveform 4. Data Setup And Hold Times, Latch Enable pulse width

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Document No.	853-0380
ECN No.	97743
Date of issue	September 27, 1989
Status	Product Specification
FAST Products	

FAST 74F621, 74F622

Transceivers

74F621 Octal Bus Transceiver, Non-Inverting (Open Collector)
74F622 Octal Bus Transceiver, Inverting (Open Collector)

FEATURES

- **High impedance NPN base inputs for reduced loading (20µA in High and Low states)**
- **Octal bidirectional bus interface**
- **Open collector outputs sink 64mA**
- **-'F621 Non-Inverting**
  -'F622 Inverting

DESCRIPTION

The 74F621 is an octal bus transceiver featuring non-inverting open collector bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA, providing very good capacitive drive characteristics. The 74F622 is a inverting version of the 74F621. These octal bus transceivers are designed for asynchronous two-way communication between data busses. The control function implementation allows for maximum flexibilty in timing. These devices allow data transmission from the A bus to the B bus or from B bus to A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the busses are effectively isolated. The dual-enable configuration gives the 'F621 and 'F622 the capability to store data by the simultaneous enabling of $\overline{OEBA}$ and OEAB.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F621	8.0ns	105mA
74F622	8.5ns	53mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F621N, N74F622N
20-Pin Plastic SOL[1]	N74F621D, N74F622D

NOTE:
1. Thermal mounting techniques are recommended.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	1.0/0.033	20µA/20µA
$\overline{OEBA}$, OEAB	Output Enable inputs	1.0/0.033	20µA/20µA
A_0- A_7	Data outputs	OC/40	OC/24mA
B_0- B_7	Data outputs	OC/106.7	OC/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

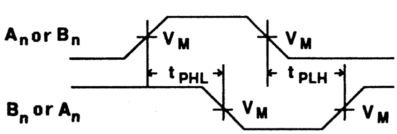
AC ELECTRICAL CHARACTERISTICS for 74F621

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	6.0 4.0	9.5 6.0	12.0 8.0	5.5 3.5	13.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	6.0 3.5	9.0 5.5	12.0 7.5	5.5 3.0	12.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEBA}$ to A_n	Waveform 3	6.0 3.5	10.0 6.5	13.5 10.5	5.5 3.0	14.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay OEAB to B_n	Waveform 4	7.0 3.5	12.0 6.5	15.0 9.5	6.0 3.0	17.0 10.0	ns

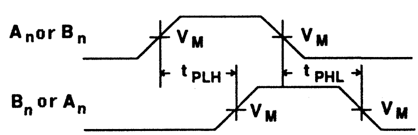
AC ELECTRICAL CHARACTERISTICS for 74F622

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	8.0 1.5	11.0 4.0	12.5 5.5	8.0 1.5	13.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	7.5 1.5	10.0 3.5	12.0 5.0	7.5 1.5	12.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEBA}$ to A_n	Waveform 3	8.0 6.0	10.5 8.0	12.0 10.0	8.0 6.0	12.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay OEAB to B_n	Waveform 4	10.0 5.0	12.5 7.5	14.5 9.0	10.0 5.0	15.5 9.5	ns

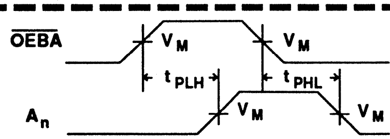
AC WAVEFORMS



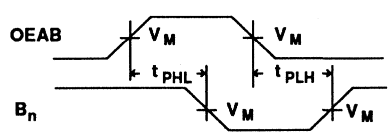
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



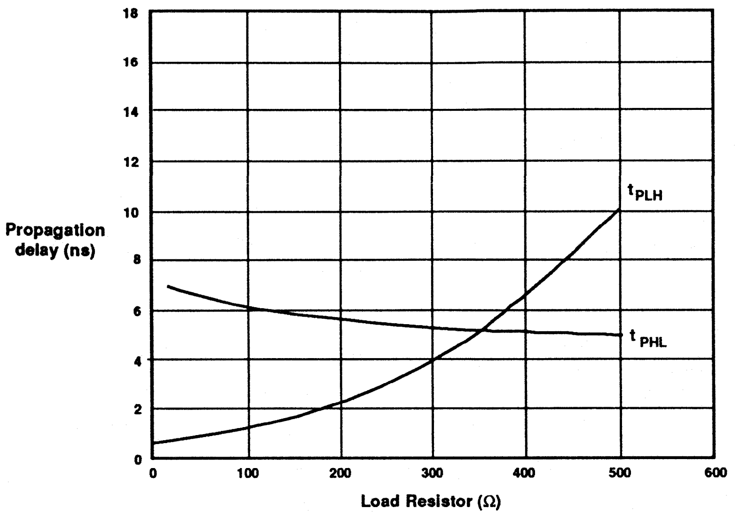
Waveform 3. Propagation delay, $\overline{OEBA}$ to An



Waveform 4. Propagation delay, OEAB to Bn

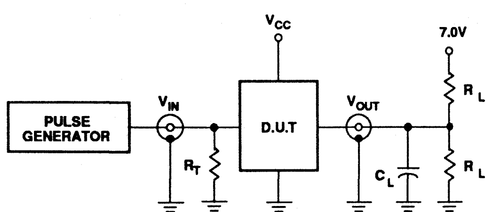
NOTE: For all waveforms, $V_M = 1.5V$.

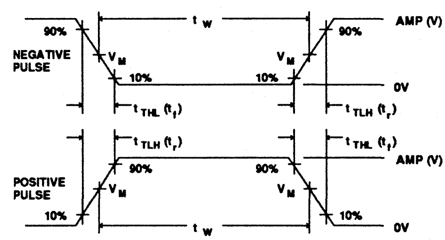
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



NOTE:
When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500 Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL} 's of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS





Test Circuit For Open Collector Outputs

V_M = 1.5V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0381
ECN No.	98171
Date of issue	November 27, 1989
Status	Product Specification
FAST Products	

FAST 74F640

Transceiver

Octal Bus Transceiver , Inverting (3-State)

FEATURES

- **High-impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Ideal for applications which require high-output drive and minimal bus loading**
- **Inverting version of 'F245**
- **Octal bidirectional bus interface**
- **3-state buffer outputs sink 64mA and source 15mA**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F640	3.5ns	78mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F640N
20-Pin Plastic SOL	N74F640D

DESCRIPTION

The 74F640 is an octal transceiver featuring inverting 3-state bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing 15mA, providing very good capacitive drive characteristics. The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receive(T/$\overline{R}$) input for direction control. The 3-state outputs, B_0-B_7, have been designed to prevent output bus loading if the power is removed from the device.

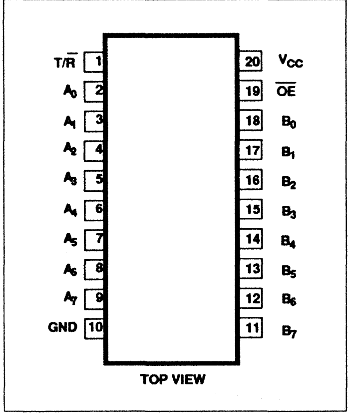
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	3.5/0.115	70μA/70μA
$\overline{OE}$	Output enable input (active Low)	2.0/0.067	40μA/40μA
T/$\overline{R}$	Transmit/Receive input	2.0/0.067	40μA/40μA
A_0- A_7	A port outputs	150/40	3.0mA/24mA
B_0- B_7	B Port outputs	750/106.7	15mA/64mA

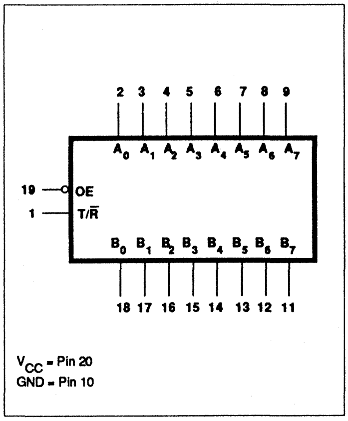
NOTE:

One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

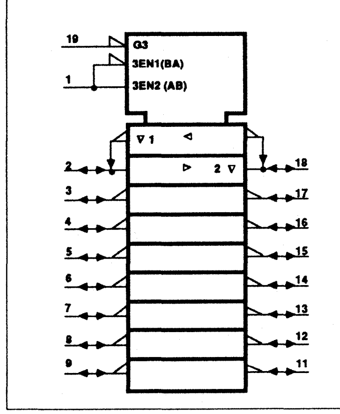
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

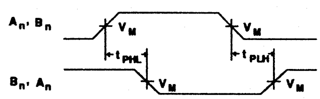


Transceiver FAST 74F640

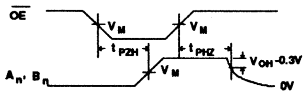
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2.0 1.0	4.5 2.5	7.0 5.0	2.0 1.0	8.0 5.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	5.5 5.5	6.5 7.0	10.5 10.5	5.0 5.0	12.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.0 2.0	3.5 4.5	6.5 7.0	1.5 2.0	8.0 7.5	ns

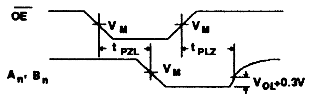
AC WAVEFORMS



Waveform 1. Propagation Delay For Inverting Outputs



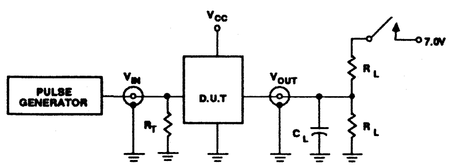
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



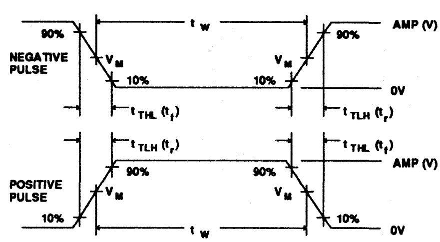
Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

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ECN No.	98172
Date of issue	November 27, 1989
Status	Product Specification
FAST Products	

FAST 74F641, 74F642
Transceivers

74F641 Octal Bus Transceiver With Common Output Enable, Non-Inverting (Open Collector)
74F642 Octal Bus Transceiver With Common Output Enable, Inverting (Open Collector)

FEATURES
- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Octal bidirectional bus interface**
- **Common Output Enable for both Transmit and Receive modes**
- **Open collector outputs sink 64mA**
- **-'F641 Non-Inverting**
  -'F642 Inverting

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F641	8.0ns	69mA
74F642	8.5ns	52mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V\pm10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74F641N, N74F642N
20-Pin Plastic SOL	N74F641D, N74F642D

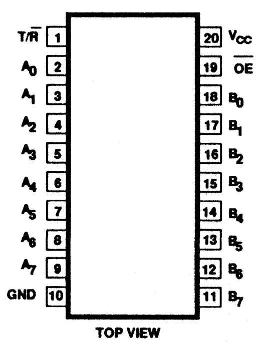
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7, B_0 - B_7	Data inputs	1.0/0.033	20μA/20μA
$T/\overline{R}$	Transmit / Receive input	2.0/0.067	40μA/40μA
$\overline{OE}$	Output Enable inputs	2.0/0.067	40μA/40μA
A_0 - A_7	Data outputs	OC/40	OC /24mA
B_0 - B_7	Data outputs	OC/106.7	OC/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC=Open Collector

PIN CONFIGURATION

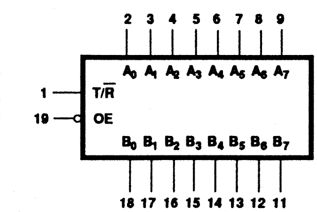
74F641



TOP VIEW

LOGIC SYMBOL

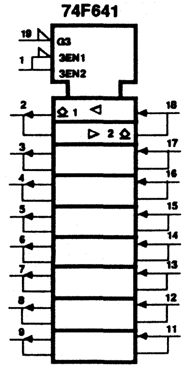
74F641



V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)

74F641



DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	μA
V_{OL}	Low-level output voltage		A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
						±5%V_{CC}		0.35	0.50	V
			B_0-B_7		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
					I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltag		T/$\overline{R}$, $\overline{OE}$	V_{CC} = 0.0V, V_I = 7.0V					100	μA
			A_n, B_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		T/$\overline{R}$, $\overline{OE}$	V_{CC} = MAX, V_I = 2.7V					40	μA
			A_n, B_n						20	μA
I_{IL}	Low-level input current		T/$\overline{R}$, $\overline{OE}$	V_{CC} = MAX, V_I = 0.5V					-40	μA
			A_n, B_n						-20	μA
I_{CC}	Supply current (total)	'F641	I_{CCH}	V_{CC} = MAX	A_n=T/$\overline{R}$=4.5V, $\overline{OE}$=GND			60	90	mA
			I_{CCL}		T/$\overline{R}$=4.5V, A_n=$\overline{OE}$=GND			78	120	mA
		'F642	I_{CCH}		A_n=T/$\overline{R}$=$\overline{OE}$=4.5V			37	55	mA
			I_{CCL}		A_n=T/$\overline{R}$=4.5V, $\overline{OE}$=GND			67	98	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

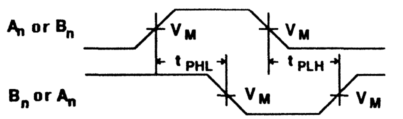
AC ELECTRICAL CHARACTERISTICS for 74F641

SYMBOL	PARAMETER	TEST CONDITION	T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	6.5 4.0	8.5 6.0	11.5 9.5	6.5 4.0	12.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	6.0 3.5	8.0 5.5	11.5 7.5	6.0 3.5	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to A_n	Waveform 4	7.0 5.0	10.5 7.0	12.5 9.0	7.0 5.0	13.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to B_n	Waveform 4	8.0 5.5	9.0 7.5	12.5 9.5	8.0 5.5	13.5 10.5	ns

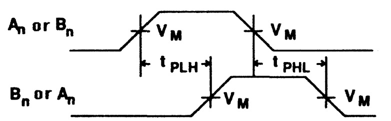
AC ELECTRICAL CHARACTERISTICS for 74F642

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	8.0 2.0	9.0 4.5	12.5 6.5	8.0 2.0	13.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	7.5 1.5	8.0 4.0	12.0 6.0	7.5 1.5	12.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to A_n	Waveform 4	7.5 6.0	9.0 8.0	12.0 10.5	7.5 6.0	12.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to B_n	Waveform 4	8.0 6.0	9.0 7.0	12.5 10.5	8.0 6.0	13.0 11.0	ns

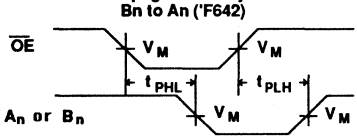
AC WAVEFORMS



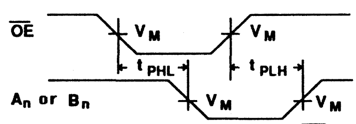
Waveform 1. Propagation delay for An to Bn or Bn to An ('F642)



Waveform 2. Propagation delay for An to Bn or Bn to An ('F641)



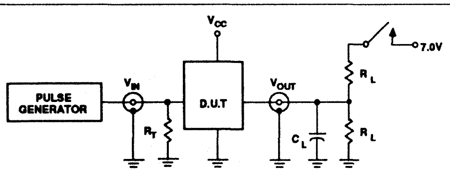
Waveform 3. Propagation delay for $\overline{OE}$ to An or Bn Outputs ('F642) (Bn or An inputs in High state)



Waveform 4. Propagation delay for $\overline{OE}$ to An or Bn Outputs ('F641) (Bn or An inputs in Low state)

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

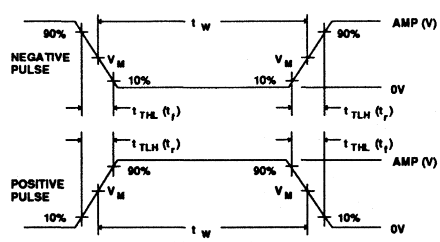
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-1124
ECN No.	99393
Date of issue	April 18, 1990
Status	Product Specification
FAST Products	

FAST 74F646, 74F646A 74F648, 74F648A Transceivers/Registers

74F646/646A Octal Transceiver/Register, Non-Inverting (3-State)
74F648/648A Octal Transceivers/Register, Inverting (3-State)

FEATURES

- **Combines 'F245 and two 'F374 type functions in one chip**
- **High impedance base inputs for reduced loading (70µA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **Controlled ramp outputs for 'F646A/'F648A**
- **3-state outputs**
- **300 mil wide 24-pin Slim Dip package**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F646/648	115MHz	140mA
74F646A/648A	185MHz	105mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F646N, N74F646AN, N74F648N, N74F648AN
24-Pin Plastic SOL[1]	N74F646D, N74F646AD, N74F648D, N74F648AD

NOTE 1: Thermal mounting techniques are recommended except for N74F646A/N74F648A.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7, B_0 - B_7	A and B inputs	3.5/0.166	70µA/70µA
CPAB	A-to-B clock input	1.0/0.033	20µA/20µA
CPBA	B-to-A clock input	1.0/0.033	20µA/20µA
SAB	A-to-B select input	1.0/0.033	20µA/20µA
SBA	B-to-A select input	1.0/0.033	20µA/20µA
DIR	Data flow Directional control enable input	1.0/0.033	20µA/20µA
$\overline{OE}$	Output Enable input	1.0/0.033	20µA/20µA
A_0 - A_7, B_0 - B_7	Outputs for 'F646A/'F648A	750/80	15mA/48mA
A_0 - A_7, B_0 - B_7	Outputs 'F646/'F648	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

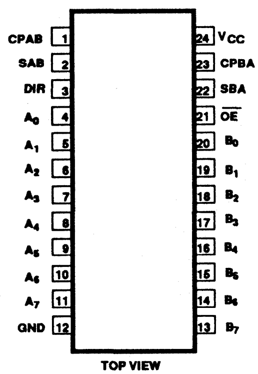
DESCRIPTION

The 74F646/646A and 74F648/648A Transceivers/Registers consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) pins determine whether data is stored or transfered through the device in real-time.The DIR determines which bus will receive data when the $\overline{OE}$ is active Low. In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses , A or B may be driven at a time. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F646/646A and 'F648/648A.

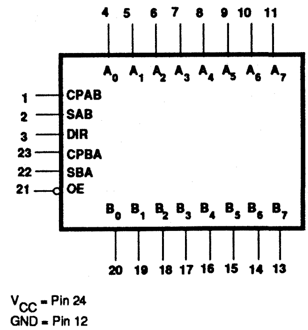
PIN CONFIGURATION

'F646/646A



LOGIC SYMBOL

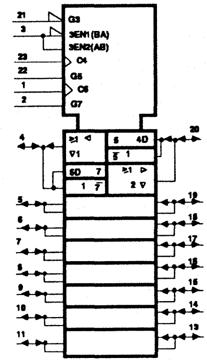
'F646/646A



V_{CC} = Pin 24
GND = Pin 12

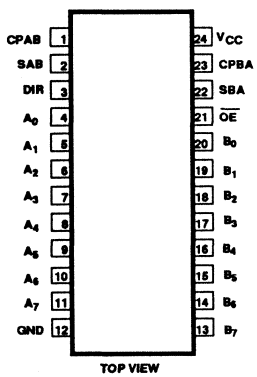
LOGIC SYMBOL(IEEE/IEC)

'F646/646A



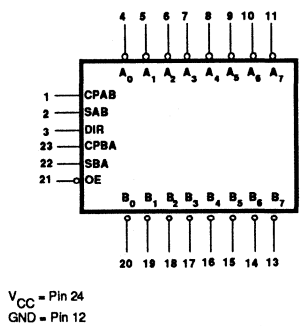
PIN CONFIGURATION

'F648/648A



LOGIC SYMBOL

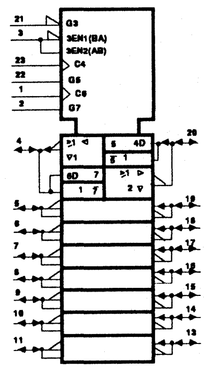
'F648/648A



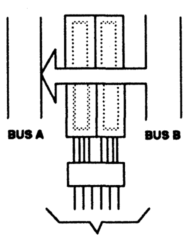
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

'F648/648A

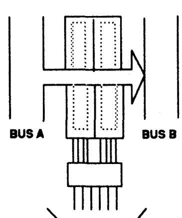


REAL TIME BUS TRANSFER
BUS B TO BUS A



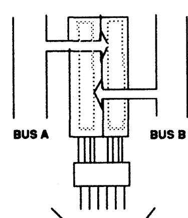
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER
BUS A TO BUS B



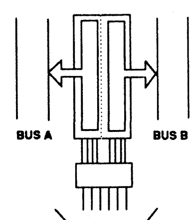
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	H	X	X	L	X

STORAGE FROM
A, B, OR A AND B



$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

TRANSFER STORED DATA
TO A OR B



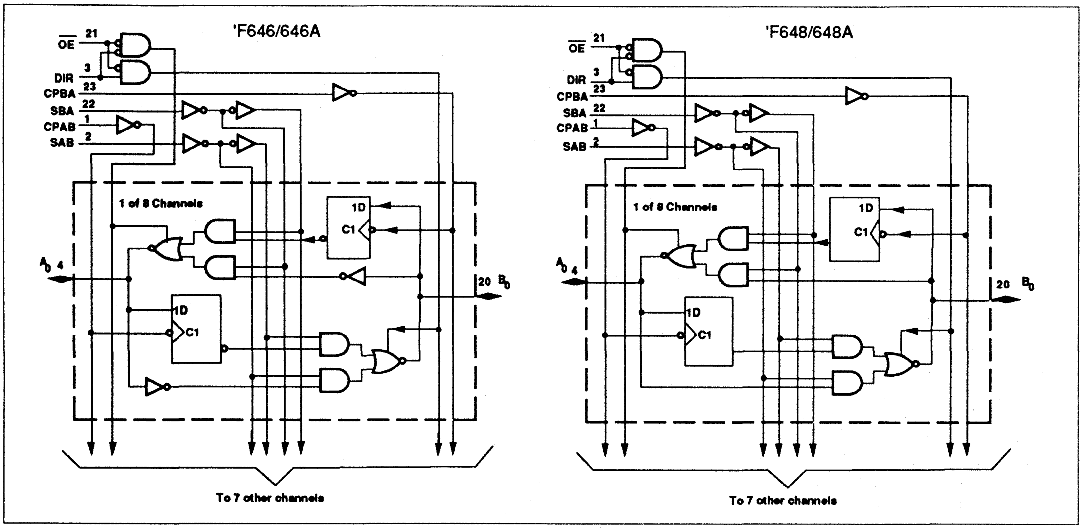
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7	'F646/646A	'F648/648A
H	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*	Store A, B unspecified*
H	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus	Real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			Stored B data to A bus	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			Stored A data to B bus	Stored $\overline{A}$ data to B bus

H= High voltage level
L= Low voltage level
X=Don't care
↑ =Low-to-High clock transition
*= The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enable, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	74F646A, 74F648A	72	mA
		74F646, 74F648	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS Min	LIMITS Nom	LIMITS Max	UNIT
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	74F646A, 74F648A			48	mA
		74F646, 74F648			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	$\pm10\%V_{CC}$	2.4			V
					$\pm5\%V_{CC}$	2.7	3.4		V
				I_{OH}=-15mA	$\pm10\%V_{CC}$	2.0			V
V_{OL}	Low-level output voltage	All	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}= 48mA	$\pm10\%V_{CC}$		0.38	0.55	V
		'F646 and 'F648 only		I_{OL}= 64mA	$\pm5\%V_{CC}$		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = MAX, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{OE}$, DIR CPAB, CPBA SAB, SBA	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
$I_{OZH} + I_{IH}$	Off-state output current, High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_O = 2.7V					70	µA
$I_{OZL} + I_{IL}$	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]	'F646, 'F648	V_{CC} = MAX			-100		-225	mA
I_O	Output current[4]	'F646A, 'F648A	V_{CC} = MAX, V_O = 2.25V			-60		-150	mA
I_{CC}	Supply current (total)	'F646 'F648 I_{CCH}	V_{CC} = MAX				125	165	mA
		'F646 'F648 I_{CCL}					160	210	mA
		'F646 'F648 I_{CCZ}					135	160	mA
		'F646A 'F648A I_{CCH}					100	145	mA
		'F646A 'F648A I_{CCL}					110	155	mA
		'F646A 'F648A I_{CCZ}					105	155	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. The output condition has been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS for 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.5 5.5	7.5 8.0	10.0 10.0	5.0 5.0	11.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	4.0 4.0	6.0 6.5	9.0 8.0	4.0 4.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2, 3	5.0 5.0	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	5.0 6.5	7.0 8.5	10.0 11.0	4.5 6.0	11.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	6.5 8.5	9.0 11.0	4.0 5.5	10.0 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	6.5 6.5	9.0 9.0	11.5 11.5	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	5.5 5.5	8.5 8.5	11.0 11.0	4.5 5.0	13.0 12.5	ns

AC SETUP REQUIREMENTS for 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.0 6.0			4.0 6.0		ns

AC ELECTRICAL CHARACTERISTICS for 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Typ	Max	$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 5.0	7.0 7.5	9.5 9.5	4.5 4.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 3	3.0 4.0	6.0 6.0	8.5 8.5	2.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2, 3	4.5 4.5	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.5 5.5	11.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.0 5.5	11.0 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	6.0 6.0	9.0 8.5	11.5 12.0	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	5.0 5.0	9.0 9.0	12.5 12.5	4.5 5.0	14.0 14.0	ns

AC SETUP REQUIREMENTS for 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Typ	Max	$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Max	UNIT
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	3.5 6.5			4.0 7.0		ns

AC ELECTRICAL CHARACTERISTICS for 74F646A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	165	185		150		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.5 4.5	7.0 7.0	10.0 9.5	4.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	4.0 2.0	6.0 5.0	9.0 8.0	3.5 2.0	10.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2, 3	4.5 3.5	6.5 8.0	9.5 10.0	4.0 3.0	10.0 11.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	3.0 3.0	5.5 5.5	9.0 9.0	2.5 2.5	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	3.0 3.5	5.0 6.0	8.0 8.5	3.0 3.0	8.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	1.5 2.5	4.0 5.5	6.5 8.0	1.0 2.0	8.0 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	2.0 3.0	4.5 5.0	7.5 8.0	1.5 2.0	8.5 8.5	ns

AC SETUP REQUIREMENTS for 74F646A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	3.5 3.5			4.5 4.0		ns

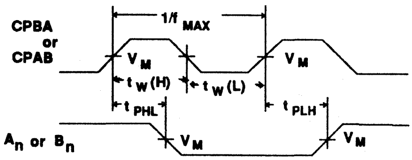
AC ELECTRICAL CHARACTERISTICS for 74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	160	185		135		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 5.5	7.0 7.5	9.5 10.0	4.5 4.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 3	2.5 4.0	4.5 6.0	7.5 8.5	2.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2, 3	4.0 4.5	7.0 7.0	9.5 9.5	3.5 4.5	11.5 10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	3.5 4.5	6.5 6.5	10.0 10.0	3.5 4.0	11.0 11.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	3.5 4.0	5.5 6.5	8.5 9.5	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	2.5 4.0	4.0 6.5	6.5 9.0	2.0 3.5	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	2.5 2.5	5.0 5.0	8.5 8.0	2.0 2.5	9.0 9.0	ns

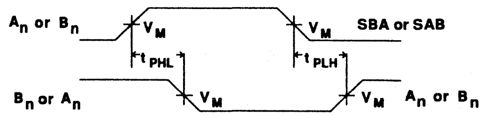
AC SETUP REQUIREMENTS for 74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	3.5 3.5			4.0 3.5		ns

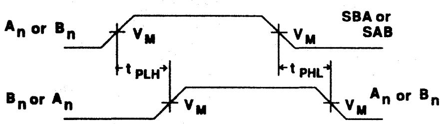
AC WAVEFORMS



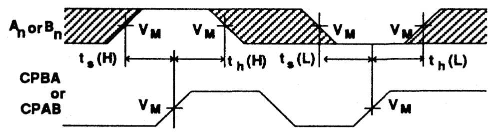
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



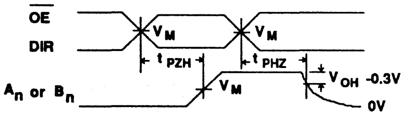
Waveform 2. Propagation Delay, An to Bn or Bn to An and SBA or SAB to An or Bn



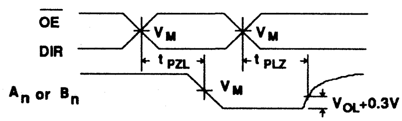
Waveform 3. Propagation Delay, An to Bn or Bn to An and SBA or SAB to An or Bn



Waveform 4. Data Setup And Hold Times



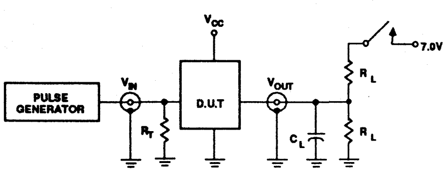
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

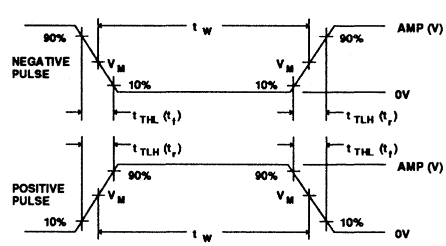
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-1126
ECN No.	98640
Date of issue	January 29, 1990
Status	Product Specification
FAST Products	

FAST 74F651, 74F651A 74F652, 74F652A Transceivers/Registers

74F651/74F651A Octal Transceiver/Register, Inverting (3-State)
74F652/74F652A Octal Transceiver/Register, Non-Inverting (3-State)

FEATURES

- **Combines 'F245 and two 'F374 type functions in one chip**
- **High impedance base inputs for reduced loading (70μA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-state outputs**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F651/74F652	110MHz	140mA
74F651A/74F652A	175MHz	110mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim Dip (300mil)[1]	N74F651N, N74F652N
24-Pin Plastic Slim Dip (300mil)	N74F651AN, N74F652AN
24-Pin Plastic SOL[1]	N74F651AD, N74F652AD

NOTE 1:
Thermal mounting techniques are recommended.

DESCRIPTION

The 74F651/74F651A and 74F652/74F652A Transceivers/Registers consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

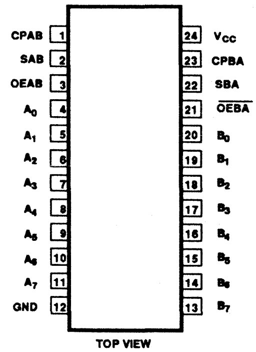
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A inputs	3.5/0.116	70μA/70μA
B_0 - B_7	B inputs	3.5/0.116	70μA/70μA
CPAB	A-to-B clock input	1.0/0.033	20μA/20μA
CPBA	B-to-A clock input	1.0/0.033	20μA/20μA
SAB	A-to-B select input	1.0/0.033	20μA/20μA
SBA	B-to-A select input	1.0/0.033	20μA/20μA
OEAB	A-to-B Output Enable input	1.0/0.033	20μA/20μA
$\overline{OEBA}$	B-to-A Output Enable input	1.0/0.033	20μA/20μA
A_0 - A_7, B_0 - B_7	A outputs ('F651, 'F652)	750/106.7	15mA/64mA
A_0 - A_7, B_0 - B_7	B outputs ('F651A, 'F652A)	750/80	15mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

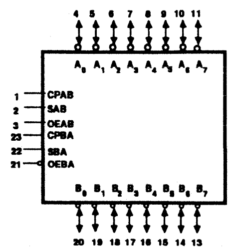
PIN CONFIGURATION

'F651/651A



LOGIC SYMBOL

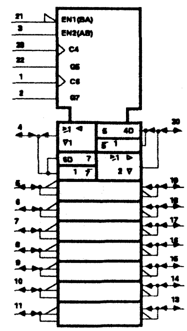
'F651/651A



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

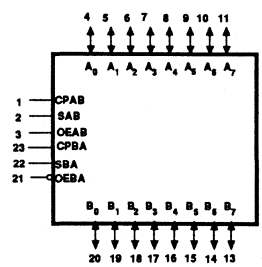
'F651/651A



The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F651/651A and 'F652/652A.
The select pins determine whether data is stored or transferred through the device in real time.
The Output Enable pins determine the direction of the data flow.

LOGIC SYMBOL

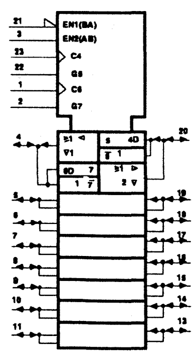
'F652/652A



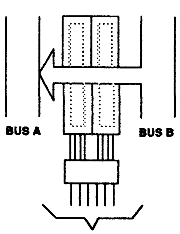
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

'F652/652A

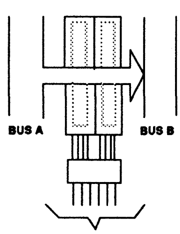


REAL TIME BUS TRANSFER BUS B TO BUS A



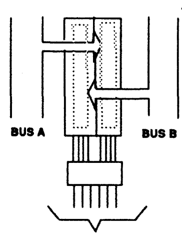
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



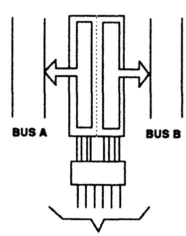
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



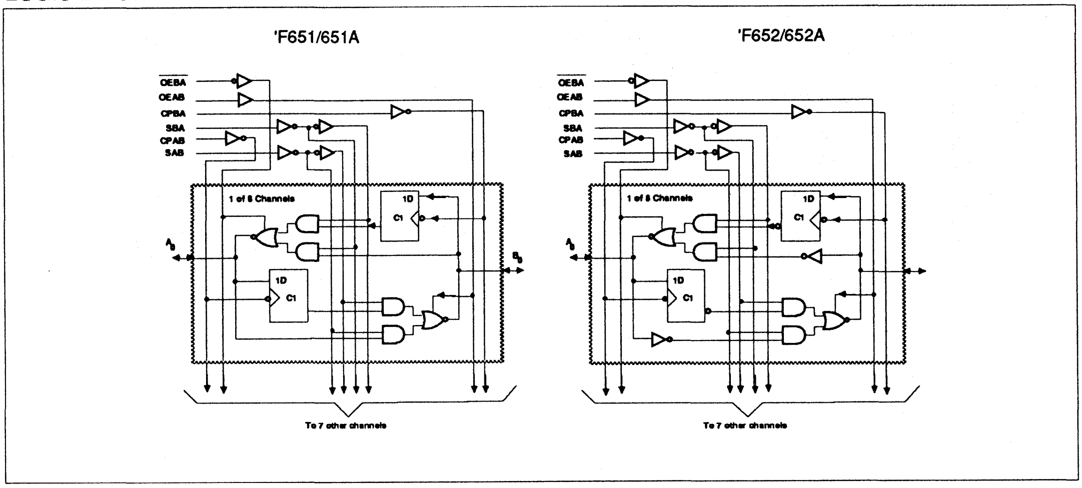
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED DATA TO A AND/OR B



OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_n	B_n	'F651/651A	'F652/652A
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B data	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, Hold B	Store A, Hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified*	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	L	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus	Real time B data to A bus
L	L	X	H or L	X	H			Stored $\overline{B}$ data to A bus	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus	Real time A data to B bus
H	H	H or L	X	H	X			Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus Stored $\overline{B}$ data to A bus	Stored A data to B bus Stored B data to A bus

NOTES:
H= High voltage level
L= Low voltage level
*= The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
↑ =Low-to-High clock transition
X=Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	'F651, 'F652	128	mA
		'F651A, 'F652A	72	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	'F651, 'F652			64	mA
		'F651A, 'F652A			48	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	Typ[2]	Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximun input voltage	others	V_{CC} =0.0V, V_I = 7.0V					100	μA
		A_0-A_7, B_0-B_7	V_{CC} =5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	OEAB, $\overline{OEBA}$, CPAB, CPBA SAB, SBA	V_{CC} =MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V					-20	μA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} =MAX, V_I= 2.7V					70	μA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} =MAX, V_I= 0.5V					-70	μA
I_{OS}	Short circuit output current[3]	74F651 74F652	V_{CC} =MAX			-100		-225	mA
I_O	Output current[4]	74F651A 74F652A	V_{CC} =MAX, V_O=2.25V			-60		-160	mA
I_{CC}	Supply current (total)	74F651 74F652 I_{CCH}	V_{CC} =MAX				110 140[5]	155 185[5]	mA
		74F651 74F652 I_{CCL}					155 165[5]	200 240[5]	mA
		74F651 74F652 I_{CCZ}					130	175	mA
		74F651A 74F652A I_{CCH}					105	145	mA
		74F651A 74F652A I_{CCL}					115	165	mA
		74F651A 74F652A I_{CCZ}					115	160	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).
5. These values are for worst case only. Worst case is defined as all (16) I/O pins selected as outputs. When using worst case conditions thermal mounting is required.

AC ELECTRICAL CHARACTERISTICS for 74F651/74F652

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	110		80		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 5.5	7.0 7.5	10.5 11.0	4.5 5.0	12.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2, 3	3.0 3.0	6.0 6.0	10.0 9.0	2.5 3.0	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2, 3	4.0 4.0	7.0 6.5	10.0 9.5	4.0 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 7 Waveform 8	4.0 6.0	7.0 10.5	10.0 12.0	3.5 5.5	11.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 7 Waveform 8	4.5 4.5	9.5 9.0	13.0 13.0	4.0 4.0	14.5 15.5	ns

AC SETUP REQUIREMENTS for 74F651/74F652

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.5			4.5 6.5		ns

Note: 1.Setup time is to protect against current surge caused by enabling 16 outputs (64mA per output) simultaneously.

AC ELECTRICAL CHARACTERISTICS for 74F651A/74F652A

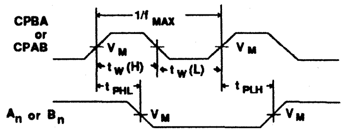
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	155	175		140		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	'F651A	Waveform 1	4.5 5.5	7.0 7.5	10.0 10.5	4.0 5.0	11.0 11.0	ns
		'F652A		5.0 5.0	7.5 7.0	10.0 10.0	4.5 4.5	11.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	'F651A	Waveform 2, 3	2.5 4.0	4.5 6.5	7.5 9.0	2.0 4.0	8.5 10.0	ns
		'F652A		4.0 3.0	6.0 5.0	9.0 8.0	3.5 2.5	10.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	'F651A	Waveform 2, 3	4.0 5.0	7.0 7.0	10.0 10.0	3.5 4.5	12.0 10.0	ns
		'F652A		4.5 4.0	7.0 8.0	10.0 10.0	4.0 4.0	11.0 11.5	ns
t_{PZH} t_{PZL}	Output Enable time OEAB or $\overline{OEBA}$ to A_n or B_n		Waveform 7 Waveform 8	3.0 3.5	5.0 6.0	8.0 8.5	2.5 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB or $\overline{OEBA}$ to A_n or B_n		Waveform 7 Waveform 8	1.5 2.5	4.0 6.0	7.0 8.5	1.0 2.0	7.5 9.0	ns

AC SETUP REQUIREMENTS for 74F651A/74F652A

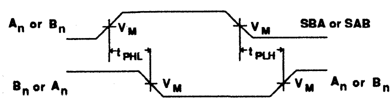
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.0 3.5			4.5 4.0		ns

Note: 1.Setup time is to protect against current surge caused by enabling 16 outputs (64mA per output) simultaneously.

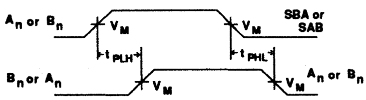
AC WAVEFORMS



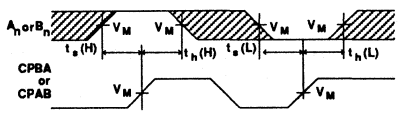
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



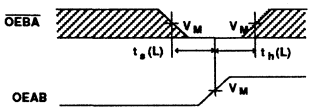
Waveform 2. Propagation Delay, An to Bn or Bn to An and SAB or SBA to An or Bn



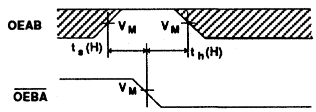
Waveform 3. Propagation Delay, An to Bn or Bn to An and SAB or SBA to An or Bn



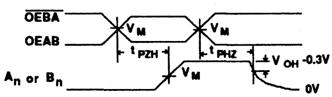
Waveform 4. Data Setup and Hold Times



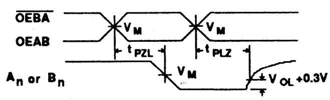
Waveform 5. OEBA to OEAB Setup and Hold Times



Waveform 6. OEAB to OEBA Setup and Hold Times



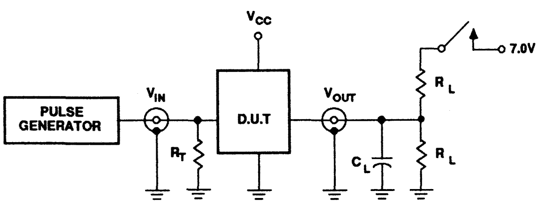
Waveform 7. 3-State Output Enable Time To High Level And Output Disable Time From High Level



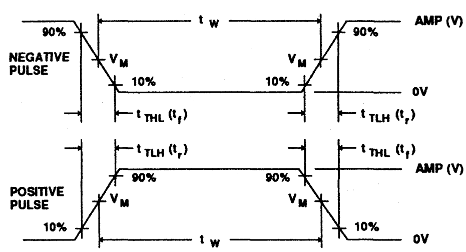
Waveform 8. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0383
ECN No.	99141
Date of issue	March 19, 1990
Status	Product Specification
FAST Products	

FAST 74F655A, 74F656A Buffers/Drivers

74F655A Octal Buffer/Driver With Parity, Inverting (3-State)

74F656A Octal Buffer/Driver With Parity, Non-Inverting (3-State)

FEATURES

- **Significantly improved AC performance over 'F655 and 'F656**
- **High impedance NPN base inputs for reduced loading (40μA in High and Low states)**
- **Ideal in applications where high output drive and light bus loading are required (I_{IL} is 40μA vs FAST std of 600μA)**
- **'F655A combines 'F240 and 'F280A functions in one package**
- **'F656A combines 'F244 and 'F280A functions in one package**
- **'F655A Inverting**
  'F656A Non-Inverting
- **3-state outputs sink 64mA and source 15mA**
- **24-pin plastic Slim DIP (300mil) package**
- **Inputs on one side and outputs on the other side simplifies PC board layout**
- **Combined functions reduce part count and enhance system performance**
- **Industrial temperature range available (-40°C to +85°C)**

DESCRIPTION

The 74F655A and 74F656A are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F655A	6.5ns	64mA
74F656A	6.5ns	64mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
24-Pin Plastic Slim DIP (300mil)	N74F655AN, N74F656AN	I74F655AN, I74F656AN
24-Pin Plastic SOL	N74F655AD, N74F656AD	I74F655AD, I74F656AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	2.0/0.066	40μA/40μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$	Output Enable inputs (active Low)	1.0/0.033	20μA/20μA
Σ_E, Σ_O	Parity outputs	750/106.7	15mA/64mA
$\overline{Q}_0$ - $\overline{Q}_7$	Data outputs ('F655A)	750/106.7	15mA/64mA
Q_0 - Q_7	Data outputs ('F656A)	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

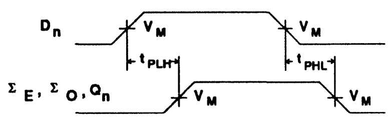
SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS Min	Typ[2]	Max	UNIT
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.3		V
					I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=64mA	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level Input current	Commercial range	D_n	V_{CC} = MAX, V_I = 2.7V					40	μA
			PI, $\overline{OE}_n$						20	μA
		Industrial range	D_n						80	μA
			PI, $\overline{OE}_n$						40	μA
I_{IL}	Low-level input current		D_n	V_{CC} = MAX, V_I = 0.5V					-40	μA
			PI, $\overline{OE}_n$						-20	μA
I_{OZH}	Off-state output current High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	Off-state output current Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)		I_{CCH}	V_{CC} = MAX				50	80	mA
			I_{CCL}					78	110	mA
			I_{CCZ}					83	90	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

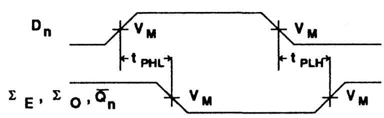
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		$T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	'F655A	Waveform 2	2.0 1.0	4.5 2.5	6.5 4.0	2.0 1.0	7.5 4.5	2.0 1.0	8.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F656A	Waveform 1	2.0 2.5	4.0 5.5	6.5 7.0	2.0 2.5	7.0 7.5	2.0 2.5	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Σ_E, Σ_O		Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	4.5 5.5	16.5 18.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	4.0 4.0	7.0 8.0	10.5 11.0	4.0 4.0	11.5 12.0	3.0 4.0	13.0 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	1.5 2.0	4.5 5.0	8.0 8.0	1.5 2.0	9.0 9.0	1.5 1.5	10.0 10.0	ns

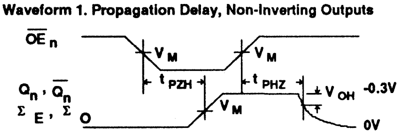
AC WAVEFORMS



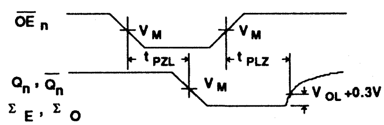
Waveform 1. Propagation Delay, Non-Inverting Outputs



Waveform 2. Propagation Delay, Inverting Outputs



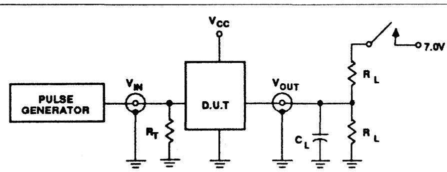
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

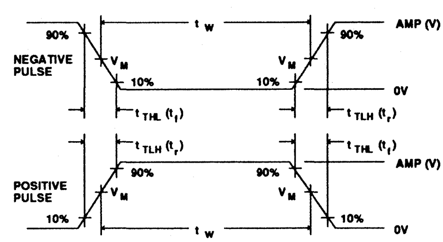
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-1125
ECN No.	
Date of issue	, 1990
Status	Product Specification
FAST Products	

FAST 74F657

Transceivers

74F657 Octal Transceivers With 8-Bit Parity Generator/Checker (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F657	8.0ns	100mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
24-Pin Plastic Slim DIP (300mil)	N74F657N	I74F657N
24-Pin Plastic SOL	N74F657D	I74F657D

NOTE:
1.Thermal mounting techniques are recommended.

FEATURES

- **Combines 74F245 and 74F280A functions in one package**
- **High impedance base input for reduced loading (70μA in High and Low states)**
- **Ideal in applications where High output drive and light bus loading are required (I_{IL} is 70μA vs FAST std of 600μA)**
- **3-state buffer outputs sink 64mA and source 15 mA**
- **Input diodes for termination effects**
- **24-pin plastic Slim Dip (300mil) package**
- **Industrial temperature range available (-40°C to +85°C)**

DESCRIPTION

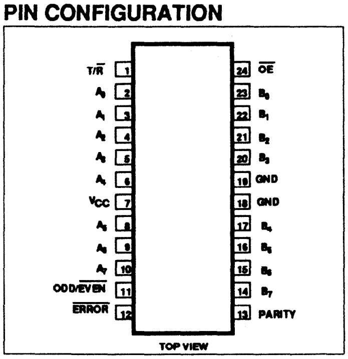
The 74F657 is an octal transceiver featuring non-inverting buffers with 3-state outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24mA at the A ports and 64mA at the B ports. The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

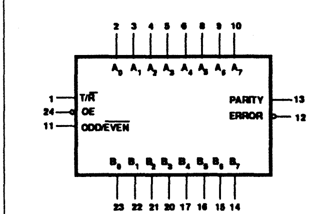
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A ports 3-state inputs	3.5/0.117	70μA/70μA
B_0 - B_7	B ports 3-state inputs	3.5/0.117	70μA/70μA
PARITY	Parity input	3.5/0.117	70μA/70μA
T/$\overline{R}$	Transmit/Receive input	2.0/0.066	40μA/40μA
ODD/$\overline{EVEN}$	Parity select input	1.0/0.033	20μA/20μA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.066	40μA/40μA
A_0 - A_7	A port 3-state outputs	150/40	3.0mA/24mA
B_0 - B_7	B port 3-state outputs	750/106.7	15mA/64mA
PARITY	Parity output	750/106.7	15mA/64mA
$\overline{ERROR}$	Error output	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

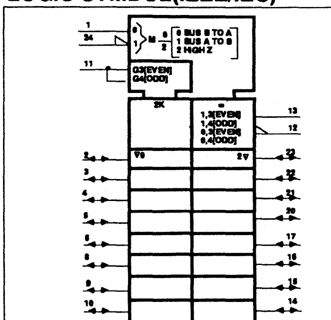


LOGIC SYMBOL



V_{CC} = Pin 7
GND = Pin 18, 19

LOGIC SYMBOL(IEEE/IEC)



Transmit (active-High) enables data from A ports to B ports; Receive (active-Low) enables data from B ports to A ports. The Output Enable ($\overline{OE}$)input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is High. The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems. The parity (PARITY) pin is an output from the generator/checker when transmitting from the port A to B (T/$\overline{R}$=High) and an input when receiving from port B to A port (T/$\overline{R}$=Low). When transmitting (T/$\overline{R}$=High) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{EVEN}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode (T/$\overline{R}$=Low) the B port is polled to determine the number of High bits. If parity select (ODD/$\overline{EVEN}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{ERROR}$ will be High, signifying no error.

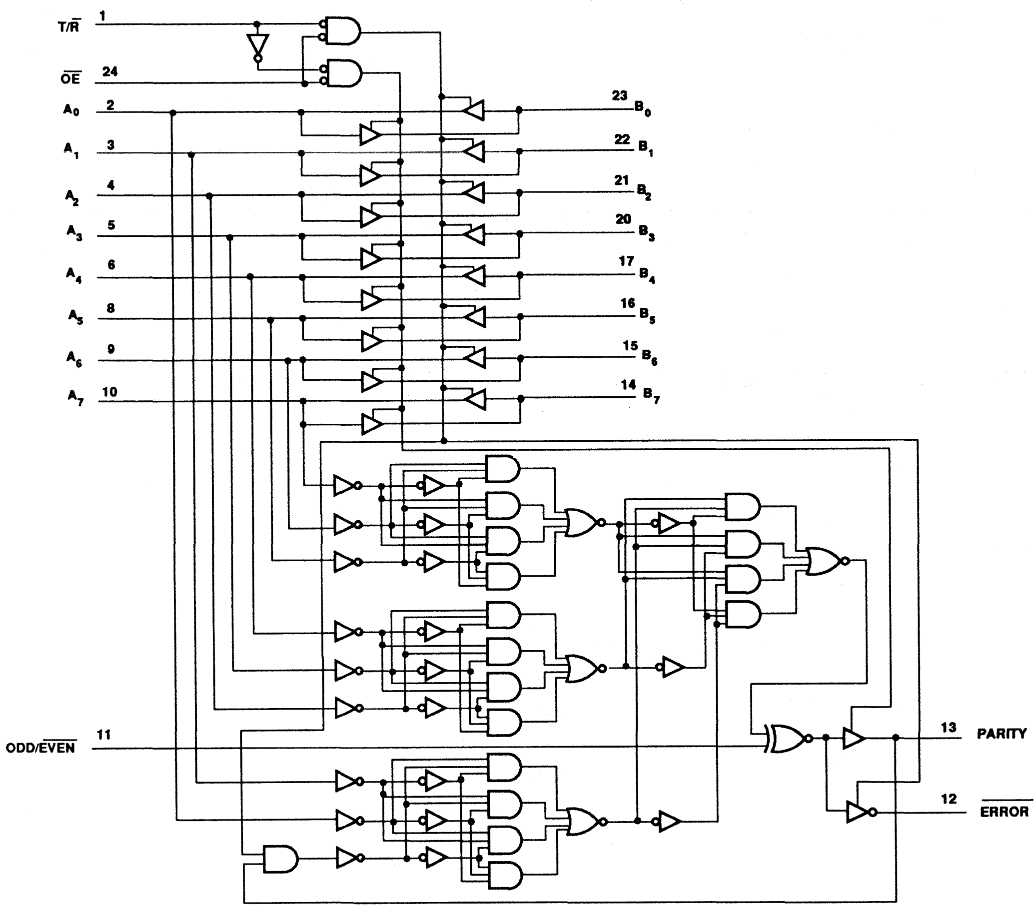
(2) even and the parity (PARITY) input is High, then $\overline{ERROR}$ will be asserted Low, indicating an error.

FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/ OUPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERROR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receivet
	L	L	H	L	L	Receive
	L	L	L	H	L	Receivet
	L	L	L	L	H	Receivett
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receivet
	L	L	H	L	H	Receive
	L	L	L	H	H	Receivet
	L	L	L	L	L	Receivett
Don't care	H	X	X	Z	Z	3-state

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



V_{CC}=Pin 7
GND=Pin 18, 19

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7, PARITY, $\overline{ERROR}$	128	mA
T_A	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7, PARITY, $\overline{ERROR}$			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7, PARITY, $\overline{ERROR}$			64	mA
T_A	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	-40		85	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	Typ[2]	Max	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA[4,5]	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B_0-B_7, PARITY, $\overline{ERROR}$		I_{OH}=-12mA[5]	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
				I_{OH}=-15mA[4]	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA[4,5]	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7, PARITY, $\overline{ERROR}$		I_{OL}=48mA[4]	±10%V_{CC}		0.38	0.55	V
				I_{OL}=48mA[5]	±5%V_{CC}		0.42	0.55	V
				I_{OL}=64mA[4]	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximun input voltage	$\overline{OE}$, $T/\overline{R}$, $ODD/\overline{EVEN}$	V_{CC} =0.0V, V_I = 7.0V					100	µA
		A_0-A_7	V_{CC} =5.5V, V_I = 5.5V					2	mA
		B_0-B_7						1	mA
I_{IH}	High-level input current	$ODD/\overline{EVEN}$	V_{CC} =MAX, V_I = 2.7V					20[4]	µA
								40[5]	µA
		$\overline{OE}$, $T/\overline{R}$						40[4]	µA
								80[5]	µA
I_{IL}	Low-level input current	$ODD/\overline{EVEN}$	V_{CC} =MAX, V_I = 0.5V					-20	µA
		$\overline{OE}$, $T/\overline{R}$						-40	µA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7, B_0-B_7 PARITY	V_{CC} =MAX, V_I= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} =MAX, V_I= 0.5V					-70	µA
I_{OZH}	Off-state output current High-level voltage applied	$\overline{ERROR}$	V_{CC} =MAX, V_I= 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} =MAX, V_I= 0.5V					-50	µA
I_{OS}	Short circuit output current[3]	A_0-A_7	V_{CC} =MAX			-60		-150	mA
		B_0-B_7				-100		-225	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} =MAX				90	125[4]	mA
							90	135[5]	mA
		I_{CCL}					106	150[4]	mA
							106	160[5]	mA
		I_{CCZ}					98	145	mA

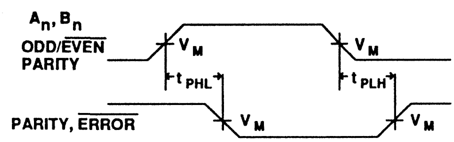
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. For commercial range.
5. For industrial range.

AC ELECTRICAL CHARACTERISTICS

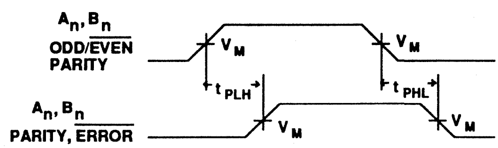
SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		LIMITS T_A = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	2.5 3.0	5.5 6.0	7.5 7.5	2.5 3.0	8.0 8.0	2.0 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to PARITY	Waveform 1,2	7.0 7.0	10.0 10.0	14.0 15.0	7.0 7.0	16.0 16.0	5.5 6.5	16.5 19.0	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{\text{EVEN}}$ to PARITY, $\overline{\text{ERROR}}$	Waveform 1,2	4.5 4.5	7.5 8.0	11.0 11.5	4.5 4.5	12.0 12.5	3.5 4.0	13.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to $\overline{\text{ERROR}}$	Waveform 1,2	8.0 8.0	14.0 14.0	20.5 20.5	7.5 7.5	22.5 22.5	7.5 7.5	24.5 25.0	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{\text{ERROR}}$	Waveform 1,2	8.0 8.0	11.5 12.0	15.5 15.5	7.5 8.0	16.5 17.0	6.5 6.5	18.5 20.0	ns
t_{PZH} t_{PZL}	Output Enable time[1] to High or Low level	Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.0 11.0	2.0 4.0	9.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.0 6.5	1.0 1.0	8.0 7.5	ns

NOTE:
1. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the $\overline{\text{ERROR}}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{\text{ERROR}}$ output . VALID data at the $\overline{\text{ERROR}}$ pin ≥ (B to A) + (A to PARITY) .

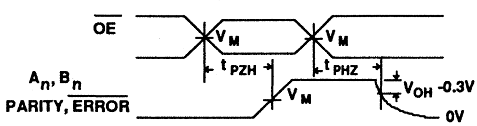
AC WAVEFORMS



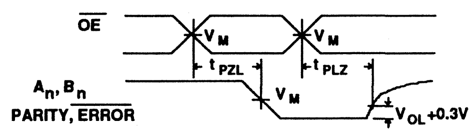
Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-Inverting Outputs



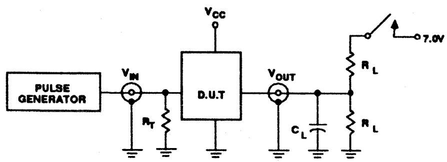
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

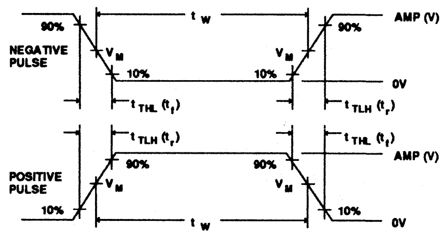
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0284
ECN No.	99394
Date of issue	April 18, 1990
Status	Product Specification
FAST Products	

FAST 74F676

Shift Register

16-Bit Serial/Parallel-In, Serial-Out Shift Register (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F676	110MHz	48mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F676N
24-Pin Plastic SOL	N74F676D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_{15}	Parallel data inputs	1.0/1.0	20μA/0.6mA
SI	Serial data input	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20μA/0.6mA
M	Mode select input	1.0/1.0	20μA/0.6mA
SO	Serial data output	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

FEATURES

- **16-bit parallel-to-serial conversion**
- **16-bit serial-in, serial-out**
- **Chip select control**
- **Power supply current 48mA typical**
- **Shift frequency 110 MHz typical**
- **Available in 300mil-wide 24-pin Slim DIP package**

DESCRIPTION

The 74F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the mode (M) input is High, information present on the parallel data (D_0 - D_{15}) inputs is entered on the falling edge of the clock pulse ($\overline{CP}$) input signal. When M is Low, data is shifted out of the most significant bit position while information present on the serial (SI) input shifts into the least significant bit position. A High signal on the chip select ($\overline{CS}$) input prevents both parallel and serial operations. The 16 bit shift register operates in one of three modes, as indicated in the shift register Function Table.

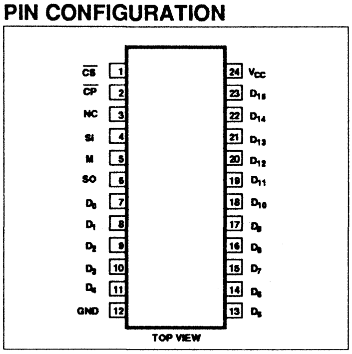
Hold : a High signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the 16 registers.

Shift/Serial load : data present on the SI pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks finally appearing on the SO pin.

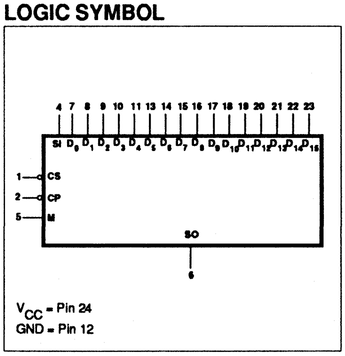
Parallel load : data present on D_0 - D_{15} are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

To prevent false clocking, $\overline{CP}$ must be Low during a Low-to-High transition of $\overline{CS}$.

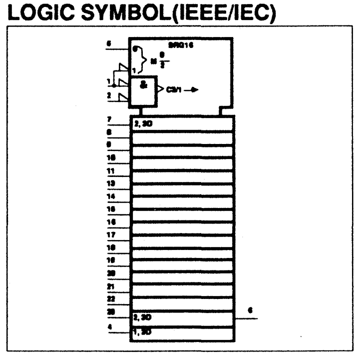
PIN CONFIGURATION



LOGIC SYMBOL

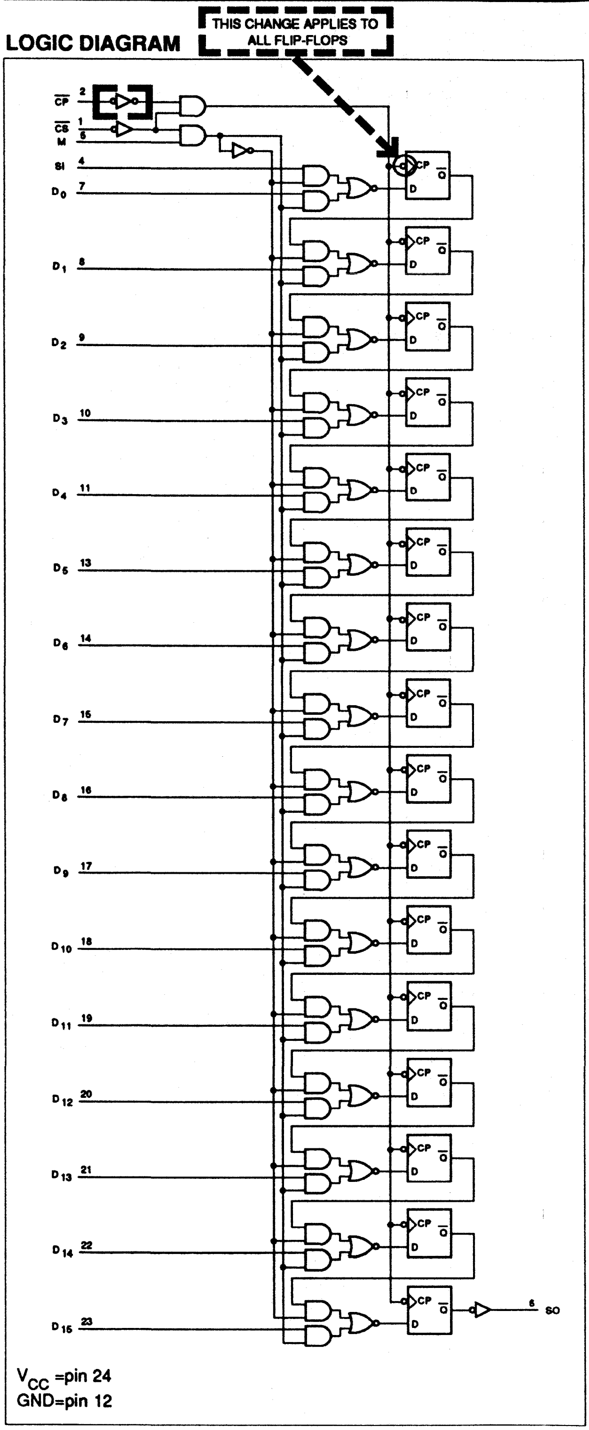


LOGIC SYMBOL(IEEE/IEC)



Shift Register FAST 74F676

LOGIC DIAGRAM



FUNCTION TABLE

CONTROL INPUTS			OPERATING MODE
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	↓	Shift/Serial load
L	H	↓	Parallel load

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low transition of clock input

Document No.	853-1368
ECN No.	99463
Date of issue	April 25, 1990
Status	Product Specification
FAST Products	

FAST 74F711/711-1, 74F712/712-1 Multiplexers

74F711 Quint 2-to-1 Data Selector Multiplexer (3-State)
74F711-1 Quint 2-to-1 Data Selector Multiplexer With 30 ohm Series Termination Resistors (3-State)
74F712 Quint 3-to-1 Data Selector Multiplexer
74F712-1 Quint 3-to-1 Data Selector Multiplexer With 30 ohm Series Termination Resistors

FEATURES for 74F711/711-1

- **Consists of five 2-to-1 Multiplexers**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **Output inverting/non-inverting option**
- **A 30 ohm series termination resistor on each output-'F711-1**
- **Outputs sink 48mA ('F711 only)**

FEATURES for 74F712/712-1

- **Consists of five 3-to-1 Multiplexers**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **A 30 ohm series termination resistor on each output-'F712-1**
- **Outputs sink 64mA ('F712 only)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F711	6.5ns	35mA
74F711-1	7.0ns	32mA
74F712	6.0ns	25mA
74F712-1	7.0ns	31mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F711N, N74F711-1N
24-Pin Plastic Slim DIP (300 mil)	N74F712N, N74F712-1N
20-Pin Plastic SOL	N74F711D, N74F711-1D
24-Pin Plastic SOL	N74F712D, N74F712-1D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F711/ 'F711-1	D_{na}, D_{nb}	Data inputs	1.0/0.066	20μA/40μA
	S	Select input	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output Enable input (active Low)	1.0/0.033	20μA/20μA
	$\overline{INV}$	Output Inverting input (active Low)	1.0/0.033	20μA/20μA
	Q_0 - Q_4	Data outputs for 'F711	750/80	15mA/48mA
	Q_0 - Q_4	Data outputs for 'F711-1	600/8.33	12mA/5mA
'F712/ 'F712-1	D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/0.066	20μA/40μA
	S_0, S_1	Select inputs	1.0/0.033	20μA/20μA
	Q_0 - Q_4	Data outputs for 'F712	750/150	15mA/64mA
	Q_0 - Q_4	Data outputs for 'F712-1	600/8.33	12mA/5mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F711/711-1 consists of five 2-to-1 multiplexers designed for address multiplexing for dynamic RAMs and other multiplexing applications. The 'F711 has a common select (S) input, an Output Enable ($\overline{OE}$) input and an Output Inverting ($\overline{INV}$) input to control the 3-state outputs. The outputs source 15mA and sink 48mA. The 'F711-1 is same as the 'F711 except that it has a 30 ohm series termination resistor on each output to reduce line noise and the 3-state outputs source 12mA and sink 5mA.

The inverting ($\overline{INV}$) input, when Low, changes data path to inverting in.

To improve speed and noise immunity, V_{CC} and GND side pins are used.

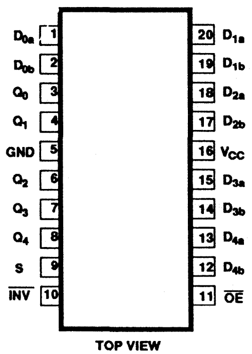
The 74F712/712-1 consists of five 3-to-1 multiplexers designed for address multiplexing for dynamic RAMs and other multiplexing applications. The 'F712 has two select (S_0,S_1) inputs to determine which set of five inputs will be propagated to the five outputs. The outputs source 15mA and sink 64mA. The 'F712-1 is same as the 'F712 except that it has a 30 ohm series termination resistor on each output to reduce line noise and the outputs source 12mA and sink 5mA.

Multiplexers

FAST 74F711/711-1, 74F712/712-1

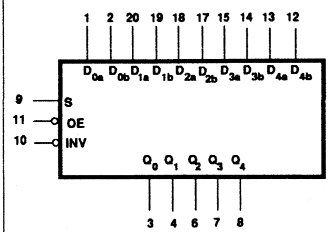
PIN CONFIGURATION

'F711/'F711-1



LOGIC SYMBOL

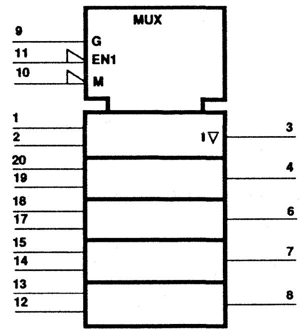
'F711/'F711-1



V_{CC} = Pin 16
GND = Pin 5

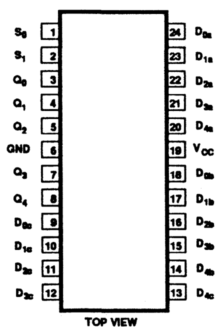
LOGIC SYMBOL(IEEE/IEC)

'F711/'F711-1



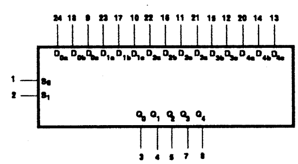
PIN CONFIGURATION

'F712/712-1



LOGIC SYMBOL

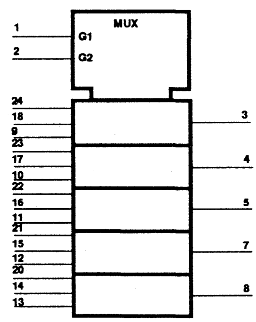
'F712/712-1



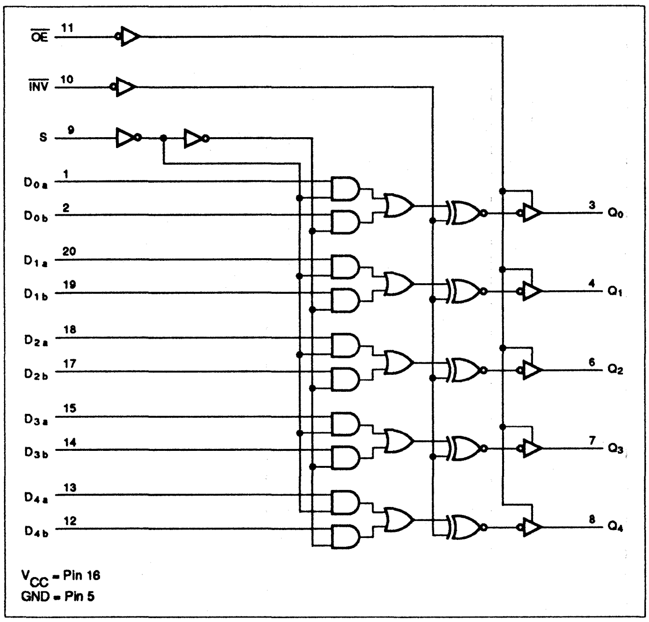
V_{CC} = Pin 19
GND = Pin 6

LOGIC SYMBOL(IEEE/IEC)

'F712/712-1



LOGIC DIAGRAM for 'F711/711-1

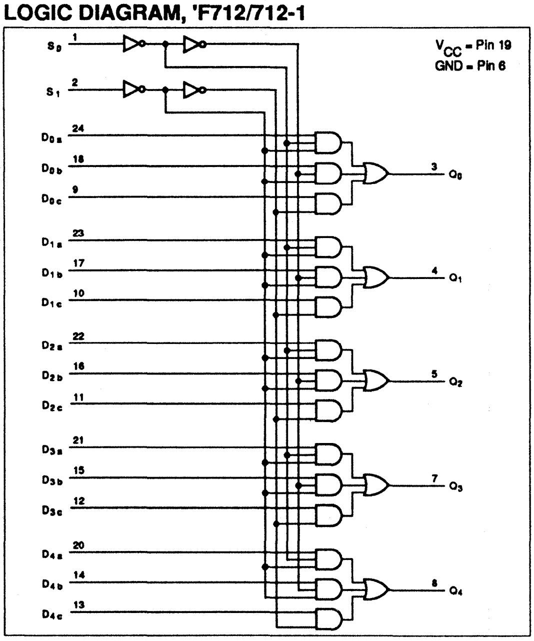


FUNCTION TABLE for 'F711/711-1

INPUTS					OUTPUT
S	$\overline{INV}$	$\overline{OE}$	D_{na}	D_{nb}	Q_n
L	L	L	data a	data b	$\overline{\text{data a}}$
H	L	L	data a	data b	$\overline{\text{data b}}$
L	H	L	data a	data b	data a
H	H	L	data a	data b	data b
X	X	H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM, 'F712/712-1



FUNCTION TABLE for 'F712/712-1

INPUTS					OUTPUT
S_0	S_1	D_{na}	D_{nb}	D_{nc}	Q_n
L	L	data a	data b	data c	data a
H	L	data a	data b	data c	data b
X	H	data a	data b	data c	data c

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	'F711	72	mA
		F712	108	mA
		'F711-1, 'F712-1	10	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	'F711, 'F712			-15	mA
		'F711-1, 'F712-1			-12	mA
I_{OL}	Low-level output current	'F711			48	mA
		'F712			64	mA
		'F711-1, 'F712-1			5	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	'F711/ 'F711-1 'F712/ 'F712-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		'F711-1/ 'F712-1 only		I_{OH}=-12mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
		'F711/ 'F712 only		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	'F711/ 'F712 only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.38	0.55	V
					±5%V_{CC}		0.42	0.55	V
		'F711-1/ 'F712-1		I_{OL}=5mA	±10%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximun input voltage		V_{CC} =MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	Others	V_{CC} =MAX, V_I = 0.5V					-20	μA
		D_n only						-40	μA
I_{OZH}	Off-state output current High-level voltage applied	'F711/ 'F711-1 only	V_{CC} =MAX, V_O= 2.7V					50	μA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} =MAX, V_O= 0.5V					-50	μA
I_{OS}	Short circuit output current[3]	'F711-1/ 'F712-1	V_{CC} =MAX			-60		-150	mA
		'F712				-100		-225	mA
I_O	Output current[4]	'F711/'F712	V_{CC} =MAX, V_O=2.25V			-60		-160	mA
I_{CC}	Supply current (total)	'F711 I_{CCH}	V_{CC} =MAX				33	45	mA
		'F711 I_{CCL}					37	50	mA
		'F711 I_{CCZ}					37	50	mA
		'F711-1 I_{CCH}	V_{CC} =MAX				30	40	mA
		'F711-1 I_{CCL}					33	45	mA
		'F711-1 I_{CCZ}					34	45	mA
		'F712 I_{CCH}	V_{CC} =MAX				20	27	mA
		'F712 I_{CCL}					30	40	mA
		'F712-1 I_{CCH}	V_{CC} =MAX				29	40	mA
		'F712-1 I_{CCL}					32	45	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3 Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

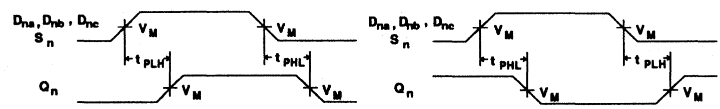
AC ELECTRICAL CHARACTERISTICS for 74F711/74F711-1

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	74F711	Waveform 1, 2	2.5 2.5	5.0 5.0	8.0 8.0	2.0 2.0	9.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Q_n	74F711	Waveform 1,3	7.0 6.0	10.5 9.5	13.0 12.5	6.0 5.5	15.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{INV}$ to Q_n	74F711	Waveform 1,3	5.5 4.5	9.0 8.5	13.0 11.5	4.5 4.0	15.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	74F711	Waveform 4 Waveform 5	2.5 3.0	5.0 5.0	7.0 7.5	2.0 3.0	7.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n	74F711	Waveform 4 Waveform 5	1.5 2.5	3.5 4.5	6.0 7.0	1.0 2.0	7.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	74F711-1	Waveform 1, 2	3.5 2.0	6.5 5.5	9.5 8.5	3.0 1.5	10.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S, $\overline{INV}$ to Q_n	74F711-1	Waveform 1,3	8.0 5.0	11.0 9.0	14.5 12.5	6.5 5.0	17.0 13.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	74F711-1	Waveform 4 Waveform 5	3.5 3.5	5.5 6.5	8.0 9.0	2.5 2.5	9.0 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n	74F711-1	Waveform 4 Waveform 5	1.0 3.0	3.5 5.5	6.5 8.0	1.0 2.5	7.5 9.5	ns

AC ELECTRICAL CHARACTERISTICS for 74F712/74F712-1

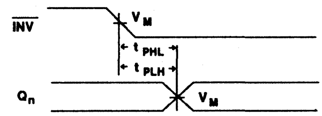
SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	74F712-1	Waveform 1, 2	2.5 2.5	5.0 5.0	8.0 8.0	2.0 2.0	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n	74F712-1	Waveform 1	8.0 6.0	10.5 9.0	13.5 12.0	7.0 6.0	16.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	74F712	Waveform 1, 2	2.0 2.0	4.0 4.0	7.5 7.5	2.0 2.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n	74F712	Waveform 1	6.5 4.5	9.5 7.5	12.5 10.5	5.5 4.0	14.5 11.0	ns

AC WAVEFORMS

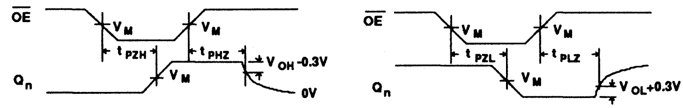


Waveform 1. Propagation Delay For Non-Inverting Output

Waveform 2. Propagation Delay For Inverting Output



Waveform 3. Propagation Delay For $\overline{INV}$ To Output

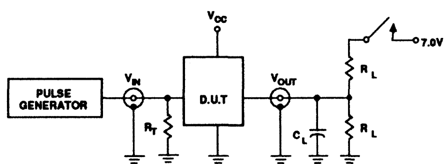


Waveform4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

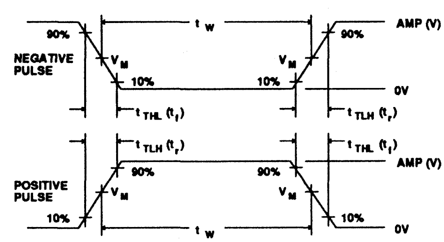
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

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Date of issue	September 20, 1989
Status	Product Specification
FAST Products	

FAST 74F723/723-1, 74F725/725-1

Multiplexers

74F723 Quad 3-to-1 Data Selector Multiplexer (3-State)
74F723-1 Quad 3-to-1 Data Selector Multiplexer With 30 ohm Series Termination Resistors (3-State)
74F725 Quad 4-to-1 Data Selector Multiplexer
74F725-1 Quad 4-to-1 Data Selector Multiplexer With 30 ohm Series Termination Resistors

FEATURES for 74F723/723-1

- **Consists of four 3-to-1 Multiplexers**
- **High impedance PNP base inputs for reduced loading (20µA in High and Low states)**
- **Inverting or non-inverting data path capability by an inverting ($\overline{\text{INV}}$) input**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **Multiple side pins for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)**
- **3-State outputs sink 48mA ('F723 only)**
- **30 ohm output series termination resistor option-74F723-1**

FEATURES for 74F725/725-1

- **Consists of four 4-to-1 Multiplexers**
- **High impedance PNP base inputs for reduced loading (20µA in High and Low states)**
- **Equivalent to two 'F253s without 3-state**
- **Outputs sink 48mA ('F725 only)**
- **30 ohm output series termination resistor option-74F725-1**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F723	6.0ns	25mA
74F723-1	7.5ns	33mA
74F725	6.0ns	20mA
74F725-1	7.0ns	20mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F723N, N74F723-1N, N74F725N, N74F725-1N
24-Pin Plastic SOL	N74F723D, N74F723-1D, N74F725D, N74F725-1D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F723/ 'F723-1	D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/0.066	20µA/40µA
	S_0, S_1	Select inputs	1.0/0.033	20µA/20µA
	$\overline{\text{INV}}$	Output Inverting input	1.0/0.033	20µA/20µA
	$\overline{\text{OE}}$	Output Enable input	1.0/0.033	20µA/20µA
'F723	Q_0 - Q_3	Data outputs	750/80	15mA/48mA
'F723-1	Q_0 - Q_3	Data outputs	600/8.33	12mA/5mA
'F725/ 'F725-1	D_{na}, D_{nb}, D_{nc}, D_{nc}	Data inputs	1.0/0.066	20µA/40µA
	S_0, S_1	Select inputs	1.0/0.033	20µA/20µA
'F725	Q_0 - Q_3	Data outputs	750/80	15mA/48mA
'F725-1	Q_0 - Q_3	Data outputs	600/8.33	12mA/5mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

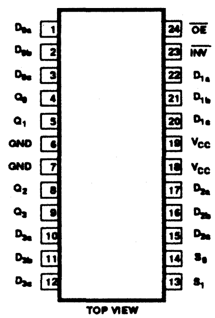
The 74F723/723-1 consists of four 3-to-1 multiplexers designed for address multiplexing for dynamic RAMs and other multiplexing applications. Select (S_0,S_1) inputs control which line is to be selected, as defined in the Function Table for 'F723/723-1. The inverting ($\overline{\text{INV}}$) input, when Low, changes data path to inverting.

To improve speed and noise immunity, V_{CC} and GND side pins are used. The 3-state outputs sorrce 15mA and sink 48mA. The 74F723-1 is same as 74F723 except that it has a 30 ohm series termination resistor on each output to reduce line noise and the 3-state outputs source 12mA and sink 5mA.

The 74F725/725-1 consists of four 4-to-1 multiplexers designed for general multiplexing purpose. The select (S_0,S_1) inputs control which line is to be selected, as defined in the Function Table for 'F725/725-1. The outputs source 15mA and sink 48mA.The 74F725-1 is same as the 74F725 except that it has a 30 ohm series termination resistor on each output to reduce line noise and the outputs source 12mA and sink 5mA.

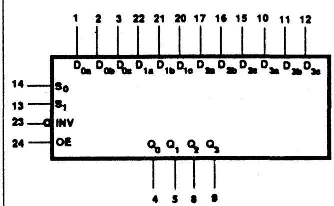
PIN CONFIGURATION

'F723/'F723-1



LOGIC SYMBOL

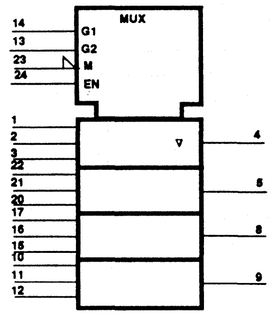
'F723/'F723-1



V_{CC} = Pin 18, 19
GND = Pin 6,7

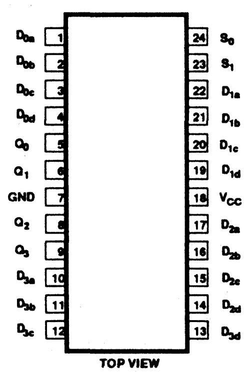
LOGIC SYMBOL(IEEE/IEC)

'F723/'F723-1



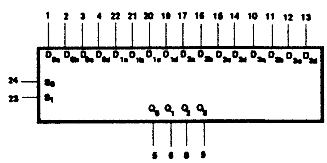
PIN CONFIGURATION

'F725/'F725-1



LOGIC SYMBOL

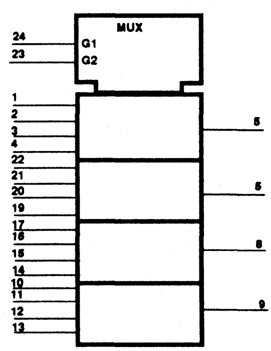
'F725/'F725-1



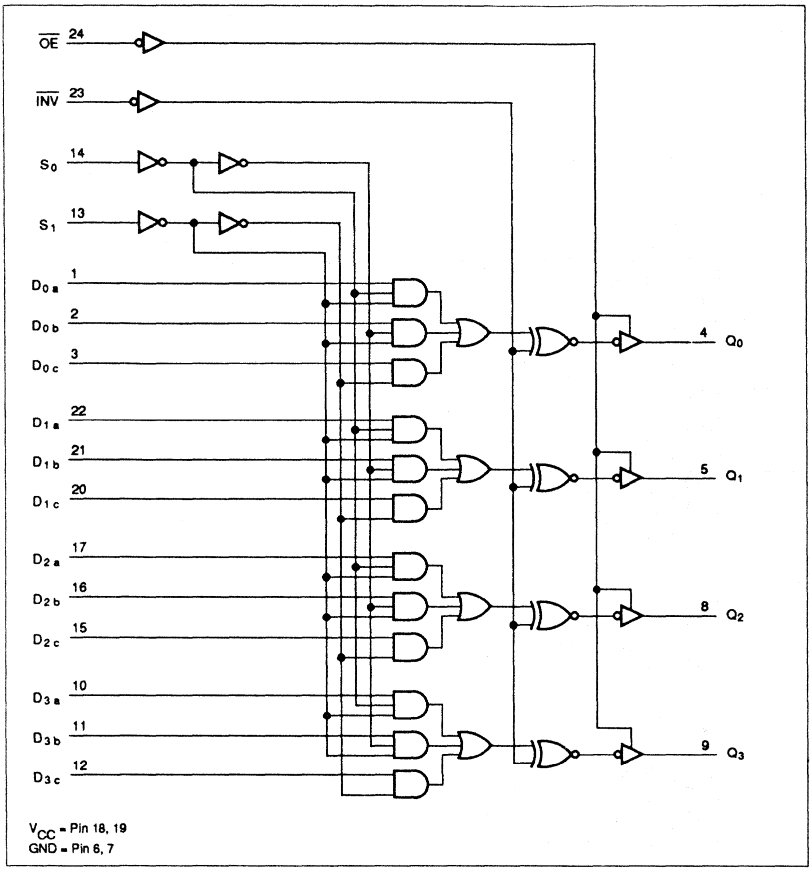
V_{CC} = Pin 18
GND = Pin 7

LOGIC SYMBOL(IEEE/IEC)

'F725/'F725-1



LOGIC DIAGRAM for 'F723/'F723-1

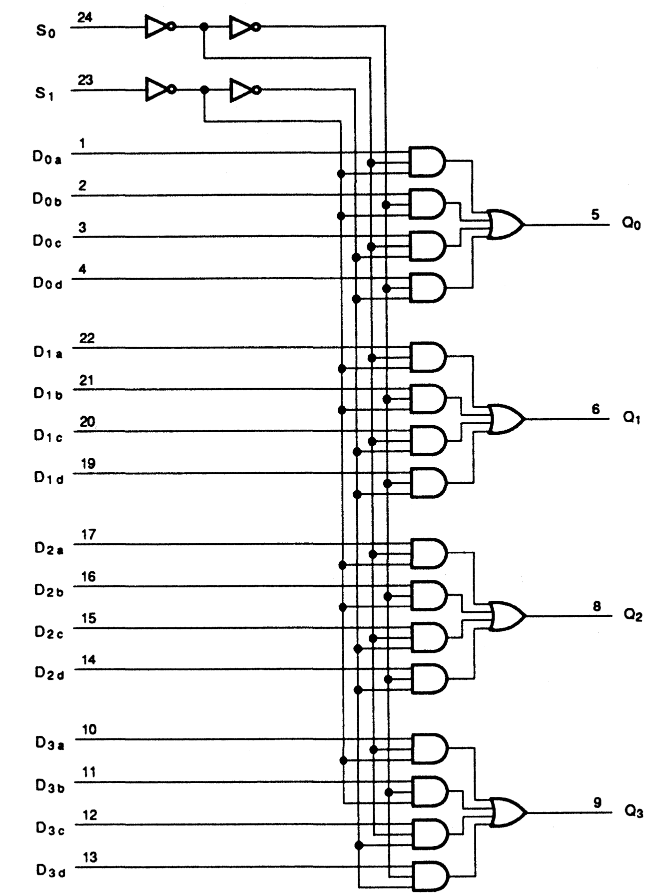


FUNCTION TABLE for 'F723/'F723-1

INPUTS							OUTPUT
S_0	S_1	$\overline{INV}$	$\overline{OE}$	D_{na}	D_{nb}	D_{nc}	Q_n
L	L	L	L	data a	data b	data c	$\overline{\text{data a}}$
L	L	H	L	data a	data b	data c	data a
H	L	L	L	data a	data b	data c	$\overline{\text{data b}}$
H	L	H	L	data a	data b	data c	data b
X	H	L	L	data a	data b	data c	$\overline{\text{data c}}$
X	H	H	L	data a	data b	data c	data c
X	X	X	H	X	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM for 'F725/'F725-1



FUNCTION TABLE for 'F725/'F725-1

INPUTS						OUTPUT
S_0	S_1	D_{na}	D_{nb}	D_{nc}	D_{nd}	Q_n
L	L	data a	data b	data c	data d	data a
H	L	data a	data b	data c	data d	data b
L	H	data a	data b	data c	data d	data c
H	H	data a	data b	data c	data d	data d

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	'F723-1, 'F725-1	10	mA
		'F723, 'F725	72	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	'F723-1, 'F725-1			-12	mA
		'F723, 'F725			-15	mA
I_{OL}	Low-level output current	'F723-1, 'F725-1			5	mA
		'F723, 'F725			48	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage	'F723/ 'F723-1 'F725/ 'F725-1		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
		'F723-1/ 'F725-1			I_{OH}=-12mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
		'F723/ 'F725			I_{OH}=-15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	'F723-1/ 'F725-1		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=5mA	±10%V_{CC}		0.38	0.55	V
						±5%V_{CC}		0.38	0.55	V
		'F723/ 'F725			I_{OL}=MAX	±10%V_{CC}		0.38	0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximun input voltage			V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} =MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	others		V_{CC} =MAX, V_I = 0.5V					-20	µA
		D_n only							-40	µA
I_{OZH}	Off-state output current High-level voltage applied	'F723/ 'F723-1 only		V_{CC} =MAX, V_O= 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied			V_{CC} =MAX, V_O= 0.5V					-50	µA
I_{OS}	Short circuit output current[3]	'F723-1/ 'F725-1		V_{CC} =MAX			-60		-150	mA
I_O	Output current[4]	'F723/'F725					-60		-160	mA
I_{CC}	Supply current	'F723	I_{CCH}	V_{CC} =MAX				23	40	mA
			I_{CCL}					25	40	mA
			I_{CCZ}					26	40	mA
		'F723-1	I_{CCH}	V_{CC} =MAX				33	45	mA
			I_{CCL}					33	45	mA
			I_{CCZ}					35	50	mA
		'F725	I_{CCH}	V_{CC} =MAX				18	30	mA
			I_{CCL}					22	35	mA
		'F725-1	I_{CCH}	V_{CC} =MAX				17	35	mA
			I_{CCL}					20	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

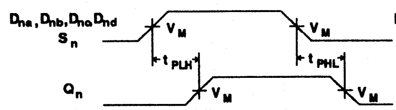
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	'F723	Waveform 1, 2	2.5 2.5	5.5 5.0	8.5 8.0	2.0 2.0	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1, $\overline{INV}$ to Q_n	'F723	Waveform 1, 2	6.0 4.5	10.0 9.0	13.5 12.5	5.0 4.0	15.0 13.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	'F723	Waveform 4 Waveform 5	2.5 3.0	4.0 5.0	7.0 8.0	2.0 3.0	7.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n	'F723	Waveform 4 Waveform 5	1.5 2.5	3.5 4.5	6.5 7.5	1.0 2.0	7.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	'F723-1	Waveform 1, 2	3.0 3.0	6.5 5.5	9.0 8.5	3.0 2.5	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1, $\overline{INV}$ to Q_n	'F723-1	Waveform 1, 2	7.0 5.0	10.5 9.5	14.0 12.5	6.0 5.0	16.0 13.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	'F723-1	Waveform 4 Waveform 5	3.0 4.0	5.0 6.0	8.0 9.0	2.5 3.5	8.5 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n	'F723-1	Waveform 4 Waveform 5	2.0 3.5	3.5 5.0	6.5 8.0	1.0 3.0	7.5 8.5	ns

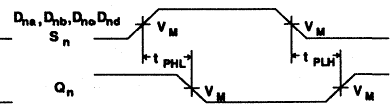
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to Q_n	'F725	Waveform 1, 2	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n	'F725	Waveform 1	6.5 5.0	9.5 8.0	12.5 11.0	5.0 5.0	14.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to Q_n	'F725-1	Waveform 1, 2	3.0 3.0	5.5 5.0	8.0 8.0	2.5 2.5	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n	'F725-1	Waveform 1	8.0 6.5	10.5 8.5	13.5 11.5	7.0 6.0	15.5 12.0	ns

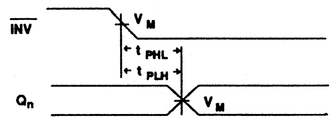
AC WAVEFORMS



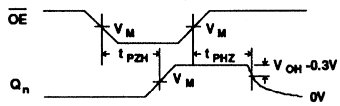
Waveform 1. Propagation Delay For Non-Inverting Output



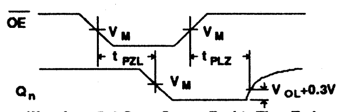
Waveform 2. Propagation Delay For Inverting Output



Waveform 3. Propagation Delay For $\overline{INV}$ To Output



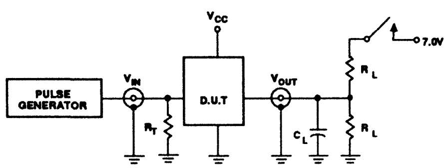
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

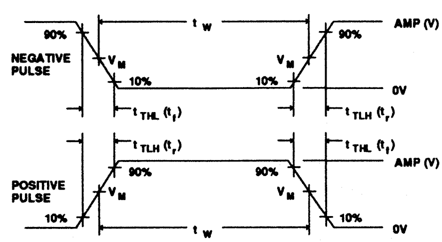
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

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ECN No.	
Date of issue	June 11, 1990
Status	Product Specification
FAST Products	

FAST 74F776

Pi-Bus Transceiver

Octal Bidirectional Latched Transceiver (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F776	6.5ns	80mA

FEATURES

- Octal Latched Transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive (100mA) open collector drivers on B-port
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with Pi-bus and IEEE 896 Futurebus Standards
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up / power down operation
- Multiple package options
- Industrial temperature range available (-40°C to +80°C)

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
28-Pin Plastic DIP (600mil)[1]	N74F776N	I74F776N
28-Pin PLCC[1]	N74F776A	I74F776A

NOTE:
1. Thermal mounting techniques are recommended.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	PNP latched inputs	3.5/0.117	70µA/70µA
B_0 - B_7	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA	A Output Enable input (active High)	1.0/0.033	20µA/20µA
$\overline{OEB}_0$, $\overline{OEB}_1$	B Output Enable inputs (active Low)	1.0/0.033	20µA/20µA
$\overline{LE}$	Latch Enable input (active Low)	1.0/0.033	20µA/20µA
A_0 - A_7	3-State outputs	150/40	3mA/24mA
B_0 - B_7	Open Collector outputs	OC*/166.7	OC*/100mA

NOTES:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
* OC = Open Collector

DESCRIPTION

The 74F776 is an octal bidirectional latched transceiver and is intended to provide the electrical interface to a high performance wired-or bus. The B port inverting drivers are low-capacitance open collector with controlled ramp and are designed to sink 100 mA from 2 volts. The B port inverting receivers have a 100 mV threshold region and a 4ns glitch filter.

The 74F776 B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (<5 pF). Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F776 A port has TTL 3-State drivers and TTL receivers with a latch function. A separate High-level control voltage input (V_x) is provided to limit the A side output level to a given voltage level (such as 3.3V). For 5.0V systems, V_x is simply tied to V_{CC}.

The 'F776 has a designed feature to control the B output transitions during power sequencing. There are two possible sequences, They are as follows:

1. When $\overline{LE}$=Low and $\overline{OEB}_n$= Low then the B outputs are disabled until the $\overline{LE}$ circuitry takes control. Then the B outputs will follow the A inputs, making a maximum of one transition during power-up (or down).
2. If $\overline{LE}$=High or $\overline{OEB}_n$= High then the B outputs will be disabled durng power-up (or down).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_A = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	5.5 6.0	7.5 7.5	12.0 10.5	5.0 6.0	12.0 11.0	5.0 6.0	12.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA_n to A_n	Waveform 3,4	8.0 8.5	10.5 12.0	14.5 14.5	7.5 8.5	15.5 17.0	7.5 8.5	15.5 17.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low OEA_n to A_n	Waveform 3,4	2.0 2.0	4.5 4.5	7.0 7.5	2.0 2.0	7.5 8.0	2.0 2.0	7.5 8.0	ns

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS T_A = +25°C V_{CC} = 5V C_D = 30pF R_U =9Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_D = 30pF R_U= 9Ω		T_A = -40°C to +85°C V_{CC} = 5V ±10% C_D = 30pF R_U = 9Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	2.0 3.5	4.0 6.0	7.0 8.0	2.0 3.0	8.0 9.0	2.0 3.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to B_n	Waveform 1	3.0 4.0	5.0 6.0	8.5 9.0	2.5 3.0	10.0 9.5	2.5 3.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEB}_n$ to B_n	Waveform 1	2.5 4.5	4.5 7.5	7.5 10.5	1.5 3.5	8.5 10.5	1.5 3.5	8.5 10.5	ns
t_{TLH} t_{THL}	Transition time, B port 1.3V to 1.7V, 1.7V to 1.3V	Test circuit and Waveform	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	4.5 4.5	0.5 0.5	4.5 4.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS T_A = +25°C V_{CC} = 5V C_L = 30pF R_L =9Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 30pF R_L = 9Ω		T_A = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time A_n to $\overline{LE}$	Waveform 2	5.0 5.0			5.0 5.0		5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time A_n to $\overline{LE}$	Waveform 2	0.0 0.0			0.0 0.0		0.0 0.0		ns
$t_w(L)$	$\overline{LE}$ Pulse width, Low	Waveform 2	6.0			6.0		6.0		ns

Document No.	853-1413
ECN No.	98963
Date of issue	February 27, 1990
Status	Product Specification
FAST Products	

FAST 74F777

Triple Bidirectional Latched Bus Transceiver

Triple Bidirectional Latched Bus Transceiver (3-State + Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F777	7ns	45mA

FEATURES

- **Latching Transceiver**
- **High drive open collector output current with minimum output swing**
- **Compatible with Test Mode (TM) Bus specification**
- **Controlled output ramp**
- **Multiple package options**

DESCRIPTION

The 74F777 is a triple bidirectional latched Bus transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. This bus has a loaded characteristic impedance range of 20 to 50 ohms and is terminated on each end with a 30 to 40 ohm resistor.

The 74F777 is a triple bidirectional transceiver with open collector B and 3-state A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100 mA from 2 volts to minimize crosstalk and ringing on the bus.

A separate output threshold clamp voltage (V_X) is provided to prevent the A port output High level from exceeding future high density processor supply voltage levels. For 5 volt systems, V_X is simply tied to V_{CC}.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP (300mil)	N74F777N
20-Pin PLCC	N74F777A

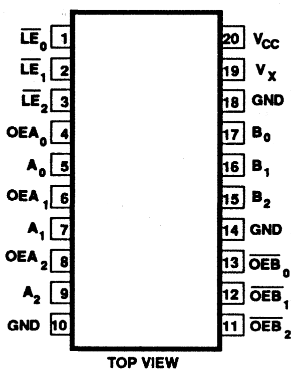
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_2	PNP latched inputs	3.5/0.117	70μA/70μA
B_0 - B_2	Data inputs with threshold circuitry	5.0/0.167	100μA/100μA
OEA_0 - OEA_2	A Output Enable inputs (active High)	1.0/0.033	20μA/20μA
$\overline{OEB}_0$ - $\overline{OEB}_2$	B Output Enable inputs (active Low)	1.0/0.033	20μA/20μA
$\overline{LE}_0$ - $\overline{LE}_2$	Latch Enable inputs (active Low)	1.0/0.033	20μA/20μA
A_0 - A_2	3-State outputs	150/40	3mA/24mA
B_0 - B_2	Open Collector outputs	OC*/166.7	OC*/100mA

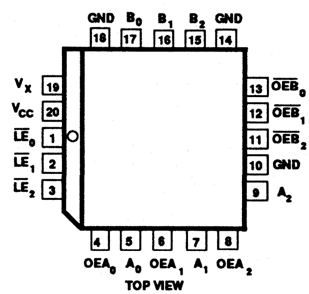
NOTES:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
* OC = Open Collector

TM-Bus Transceiver FAST 74F777

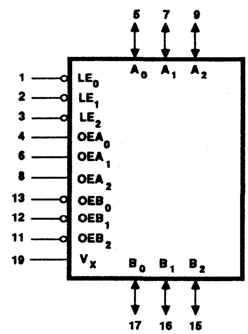
PIN CONFIGURATION



PIN CONFIGURATION PLCC

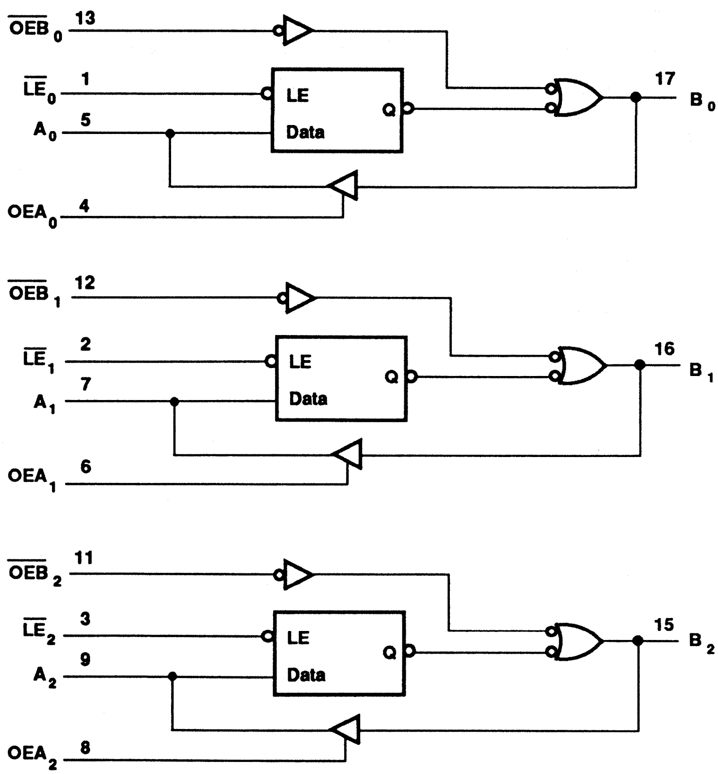


LOGIC SYMBOL



V_{CC} = Pin 20 V_X = Pin 19
GND = Pin 10,14, 18

LOGIC DIAGRAM



V_{CC} = Pin 20 V_X = Pin 19
GND = Pin 10, 14, 18

FUNCTION TABLE

INPUTS					LATCH	OUTPUTS		OPERATING MODE
A_n	B_n*	$\overline{LE}_n$	OEA_n	$\overline{OEB}_n$	STATE	A_n	B_n	
H	X	L	L	L	H	Z	H**	A 3-state, Data from A to B
L	X	L	L	L	L	Z	L	
X	X	H	L	L	Q_n	Z	Q_n	A 3-state, Latched data to B
–	–	L	H	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	$H^{(2)}$	H	$Z^{(2)}$	Preconditioned Latch enabling data transfer from B to A
–	L	H	H	L	$H^{(2)}$	L	$Z^{(2)}$	
–	–	H	H	L	Q_n	Q_n	Q_n	Latch state to A and B
H	X	L	L	H	H	Z	Z	B and A 3-state
L	X	L	L	H	L	Z	Z	
X	X	H	L	H	Q_n	Z	Z	
–	H	L	H	H	H	H	Z	B 3-state, Data from B to A
–	L	L	H	H	L	L	Z	
–	H	H	H	H	Q_n	H	Z	
–	L	H	H	H	Q_n	L	Z	

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High Impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB}_0$ and $\overline{OEB}_1$ are Low and $\overline{LE}$ is High.
B* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to Low state.
H** = Goes to level of pullup voltage.
NOTE = Each latch is independent. The latches may be run in any combination of modes.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_X	Threshold control		-0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	-0.5 to +7.0	V
		A_0 - A_2, B_0 - B_2	-0.5 to 5.5	
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	A_0 - A_2	48	mA
		B_0 - B_2	200	
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except B_0 - B_2	2.0			V
		B_0 - B_2	1.6			
V_{IL}	Low-level input voltage	Except B_0 - B_2			0.8	V
		B_0 - B_2			1.43	
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0 - A_2			-3	mA
I_{OL}	Low-level output current	A_0 - A_2			24	mA
		B_0 - B_2			100	
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	Typ[2]	Max	UNIT
I_{OH}	High level output current	B_0 - B_2	V_{CC} = MAX, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	μA
I_{OFF}	Power-off output current	B_0 - B_2	V_{CC} = 0.0V, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	μA
V_{OH}	High-level output voltage	A_0 - A_2[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA, V_X = V_{CC}	2.5		V_{CC}	V
				I_{OH} = -0.4mA, V_X = 3.13V & 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	A_0 - A_2[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA, V_X = V_{CC}			0.5	V
		B_0 - B_2	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA			1.15	V
				I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A_0 - A_2	V_{CC} = MIN, I_I = I_{IK}				-0.5	V
		Except A_0 - A_2	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	V_{CC} =MAX, V_I = 7.0V				100	μA
		A_0 - A_2, B_0 - B_2	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High-level input current	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	V_{CC} = MAX, V_I = 2.7V, B_n - A_n = 0V				20	μA
		B_0 - B_2	V_{CC} = MAX, V_I = 2.1V				100	μA
I_{IL}	Low-level input current	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	V_{CC} = MAX, V_I = 0.5V				-20	μA
		B_0 - B_2	V_{CC} = MAX, V_I = 0.3V				-100	μA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0 - A_2	V_{CC} = MAX, V_O =2.7V				70	μA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	A_0 - A_2	V_{CC} = MAX, V_O =0.5V				-70	μA
I_X	High-level control current		V_{CC} = MAX, V_X = V_{CC}, $\overline{LE}$ = OEA_n = $\overline{OEB}_n$ = 2.7V, A_0 - A_2= 2.7V, B_0 - B_2 = 2.0V		-100		100	μA
			V_{CC} = MAX, V_X = 3.13V & 3.47 V, $\overline{LE}$ = OEA_n = 2.7V, $\overline{OEB}_n$ =A_0 - A_7 = 2.7V, B_0 - B_2 = 2.0V		-10		10	mA
I_{OS}	Short-circuit output current[3]	A_0 - A_2 only	V_{CC} = MAX, B_n = 1.8V, OEA_n = 2.0V, $\overline{OEB}_n$ = 2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			40	60	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			55	80	mA
		I_{CCZ}	V_{CC} = MAX, V_{IL} = 0.5V			45	67	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH}=1.8V and V_{IL} =1.3V.

AC ELECTRICAL CHARACTERISTICS

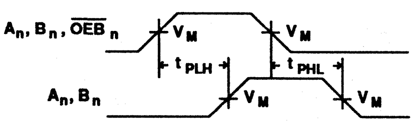
SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			A PORT LIMITS T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	8.5 7.5	10.5 9.5	13.0 12.0	8.0 7.5	14.5 12.5	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA_n to A_n	Waveform 3,4	8.0 9.0	10.0 11.0	13.0 14.0	7.0 8.0	14.5 15.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA_n to A_n	Waveform 3,4	1.5 1.5	3.0 3.0	6.0 6.0	1.0 1.0	6.5 6.0	ns

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS T_A = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			B PORT LIMITS T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_D = 30pF, R_U = 9Ω		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	3.0 5.0	4.5 6.5	7.0 9.0	2.5 4.5	8.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}_n$ to B_n	Waveform 1	3.5 5.5	5.5 7.5	8.0 10.5	3.0 5.0	9.0 11.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}_n$ to B_n	Waveform 1	3.0 6.0	5.0 8.0	7.5 10.5	3.0 5.5	8.0 12.0	ns
t_{TLH} t_{THL}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveform	0.5 0.5	4.0 2.0	4.5 4.5	0.5 0.5	7.0 4.5	ns

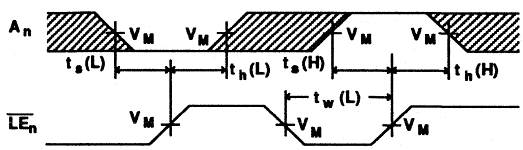
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 30pF, R_U = 9Ω			LIMITS T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 30pF, R_U = 9Ω		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time A_n to $\overline{LE}_n$	Waveform 2	4.0 4.5			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time A_n to $\overline{LE}_n$	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_w(L)$	$\overline{LE}_n$ Pulse width, Low	Waveform 2	5.5			6.5		ns

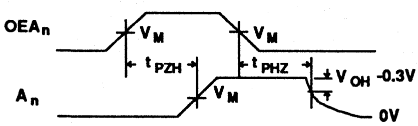
AC WAVEFORMS



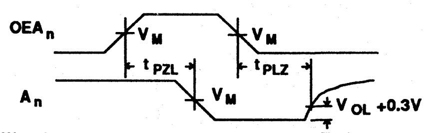
Waveform 1. Propagation Delay For Data To Output And Enable/Disable Time OEB$_n$ To B$_n$



Waveform 2. Data Setup And Hold Times And LE Pulse Width



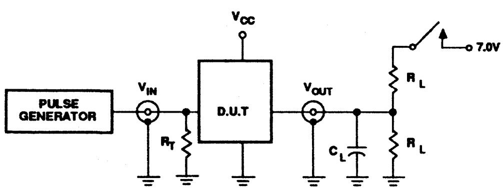
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



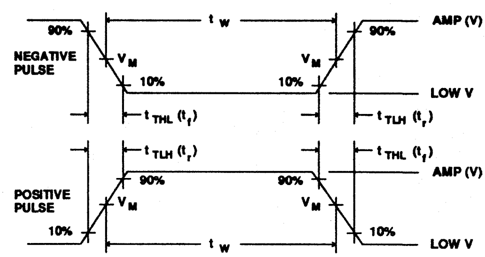
Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs On A Port

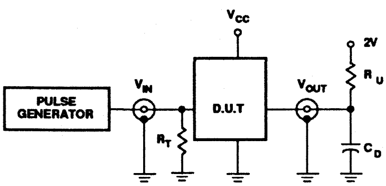


$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit For Outputs On B Port

FAMILY 74F	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

Document No.	853-0385
ECN No.	97676
Date of issue	September 20, 1989
Status	Product Specification
FAST Products	

FAST 74F779 Counter

8-Bit Bidirectional Binary Counter (3-state)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F779	145MHz	90mA

FEATURES

- **Multiplexed 3-state I/O ports for bus oriented applications**
- **Built-in look-ahead carry capability**
- **Center power pins to reduce effects of package inductance**
- **Count frequency 145MHz typical**
- **Supply current 90mA typical**
- **See 'F269 for 24 pin separate I/O port version**
- **See 'F579 for 20 pin version**
- **See 'F1779 for extended function version of the 'F799**

DESCRIPTION

The 74F779 is fully synchronous 8-stage Up/Down Counter with multiplexed 3-state I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0,S_1). The device also features carry look-ahead for easy cascading. All state changes are initiated by the rising edge of the clock. When $\overline{CET}$ is High the data outputs are held in their current state and $\overline{TC}$ is held High. The $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

ORDERING INFORMATION

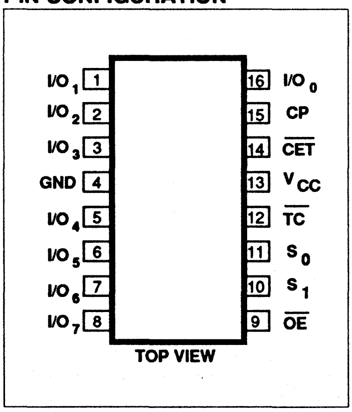
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F779N
16-Pin Plastic SOL	N74F779D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

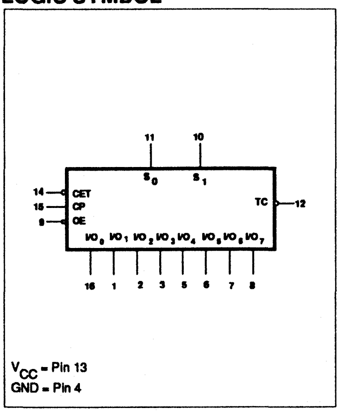
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Data inputs	3.5/1.0	70µA/0.6mA
	Data outputs	150/40	3.0mA/24mA
S_0, S_1	Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

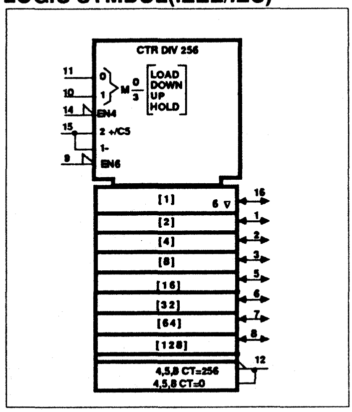
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Document No.	853-1269
ECN No.	97741
Date of issue	September 27, 1989
Status	Product Specification
FAST Products	

FAST 74F786

Asynchronous Bus Arbiter

4-Bit Asynchronous Bus Arbiter

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N74F786	6.6ns	55mA

FEATURES

- **Arbitrates between 4 asynchronous inputs**
- **Separate grant output for each input**
- **Common output enable**
- **On-board 4 input AND gate**
- **Metastable-free outputs**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F786N
16-Pin Plastic SO	N74F786D

DESCRIPTION

The 74F786 is an asynchronous 4-bit arbiter designed for high speed real-time applications. The priority of arbitration is determined on a first-come first-served basis. Separate Bus Grant ($\overline{BG}_n$) outputs are available to indicate which one of the request inputs is served by the arbitration logic. All $\overline{BG}$ outputs are enabled by a common enable ($\overline{EN}$) pin. In order to generate a bus request signal a separate 4 input AND gate is provided which may also be used as an independent AND gate. Unused Bus Request ($\overline{BR}_n$) inputs may be disabled by tying them High.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{BR}_0$ - $\overline{BR}_3$	Bus Request inputs (active Low)	1.0/3.0	20µA/1.8mA
A, B, C, D	AND gate inputs	1.0/1.0	20µA/0.6mA
$\overline{EN}$	Common Bus Grant output enable input (active Low)	1.0/1.0	20µA/0.6mA
Y_{OUT}	AND gate output	150/40	3.0mA/24mA
$\overline{BG}_0$ - $\overline{BG}_3$	Bus Grant outputs (active Low)	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

The 'F786 is designed so that contention between two or more request signals will not glitch or display a metastable condition. In this situation an increase in the $\overline{BR}_n$ to $\overline{BG}_n$ t_{PHL} may be observed. A typical 'F786 has an h = 6.6ns, τ = .41ns and and T_0 = 5µsec.

Where:

h= Typical propagation delay through the device and τ and T_0 are device parameters derived from test results and can most nearly be defined as:

τ= A function of the rate at which a latch in a metastable state resolves that condition.

T_0= A function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a very strong function of the normal propagation delay of the device.

For further information, please refer to the 'F786 application notes.

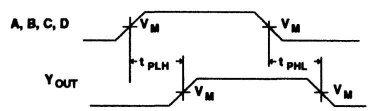
The $\overline{BR}_n$ inputs have no inherent priority. The arbiter assigns priority to the incoming requests as they are received, therefore, the first $\overline{BR}$ asserted will have the highest priority. When a bus request is received its corresponding bus grant becomes active, provided that $\overline{EN}$ is Low. If additional bus requests are made during this time they are queued. When the first request is removed, the arbiter services the bus request with the next highest priority. Removing a request while a previous request is being serviced can cause a grant to be changed when arbitrating between three or four requests. For that reason, the user should not remove ungranted requests when arbitrating between three or four requests. This does not apply to arbitration between two requests.

If two or more $\overline{BR}_n$ inputs are asserted at precisely the same time, one of them will be selected at random, and all $\overline{BG}_n$ outputs will be held in the High state until the selection is made. This guarantees that an erroneous $\overline{BG}_n$ will not be generated even though a metastable condition may occur internal to the device.
When the $\overline{EN}$ is in the High state the $\overline{BG}_n$ outputs are forced High.

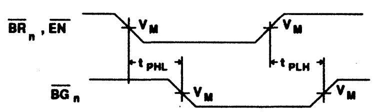
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay, A, B, C, D to Y_{OUT}	Waveform 1	2.5 2.5	4.5 4.5	7.5 7.5	2.0 2.5	8.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{BR}_n$ to $\overline{BG}_n$	Waveform 2	5.0 4.5	7.0 6.5	10.0 9.5	4.5 4.0	10.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{EN}$ to $\overline{BG}_n$	Waveform 2	3.0 2.5	5.0 4.5	8.0 7.5	2.5 2.5	8.5 8.0	ns
t_{PHL}	Propagation delay, $\overline{BR}_a$ to $\overline{BG}_b$	Waveform 3	5.0	7.0	10.0	4.5	10.5	ns

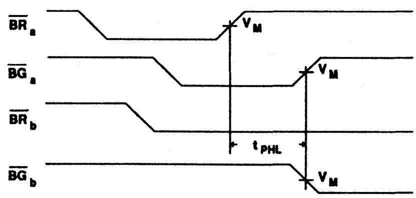
AC WAVEFORMS



Waveform 1. AND Gate Input to Output Delays



Waveform 2. Bus Request or Enable to Bus Grant Delays

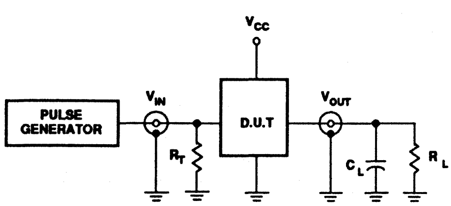


Waveform 3. Bus Request to Bus Grant Delay

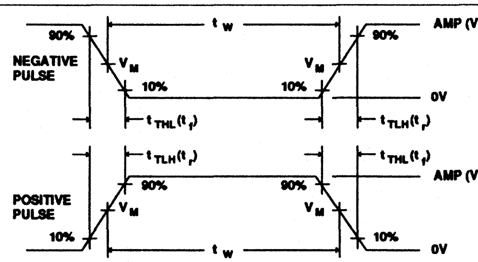
NOTE: a and b represent any of the Bus Requests or Grants. $\overline{BG}_a$ Low-to-High transition and the $\overline{BG}_b$ High-to-Low transition occur simultaneously.

For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-1421
ECN No.	99465
Date of issue	April 25, 1990
Status	Product Specification
FAST Products	

FAST 74F807

Octal Shift/Count Registered Transceiver with Adder and Parity (3-State)

FEATURES

- **High speed parallel registers with positive edge-triggered D-type flip-flops**
- **High speed full adder**
- **8-bit parity generator**
- **High impedance PNP inputs for light bus loading**
- **Center V_{CC} and GND pins and controlled output buffers minimize ground-bounce problems**
- **3-state outputs glitch free during power-up and power-down**
- **Broadside pinout**

DESCRIPTION

The 74F807 Octal Bus, Shift/Count Transceiver is designed to input data from either the A or B ports to an internal storage register. This data can then be shifted left with serial or parallel outputs, added to additional data that appears on the A-input with Carry In and Carry Out bits, incremented by the Clock Input or incremented by the Clock enabled with Carry In. An 8-bit odd parity generator is attached to the register Q Outputs.

The data in the storage register can be presented on either the A or B ports for output.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F807	115MHz	155mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (300 mils)[1]	N74F807N
28-Pin SOL[2]	N74F807D
28-Pin PLCC	N74F807A

NOTE:
1. To be released in May, 1990
2. Thermal mounting techniques are recommended.

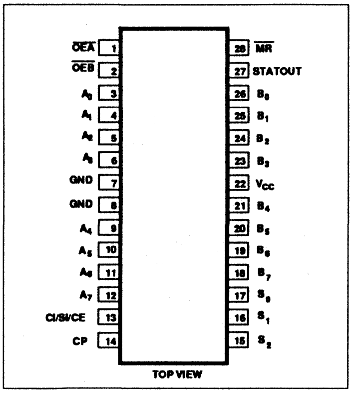
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_n, B_n	Data I/O inputs	3.5/0.166	70μA/70μA
$\overline{OEA}$, $\overline{OEB}$	Output Enable inputs	1.0/0.033	20μA/20μA
CI/SI/CE	Carry/Serial/Clock Enable input	1.0/0.033	20μA/20μA
CP	Clock input	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset input	1.0/0.033	20μA/20μA
S_n	Select inputs	1.0/0.033	20μA/20μA
STATOUT	Status Out output	150/40	3.0mA/24mA
A_n, B_n	Data I/O outputs	150/40	3.0mA/24mA

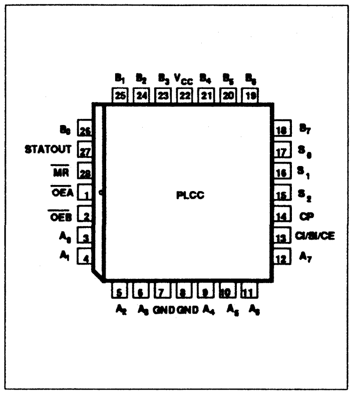
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

Octal Shift/Count Transceiver FAST 74F807

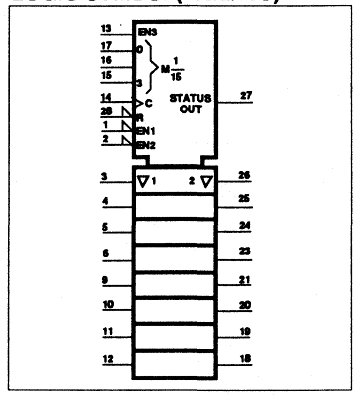
DIP PIN CONFIGURATION



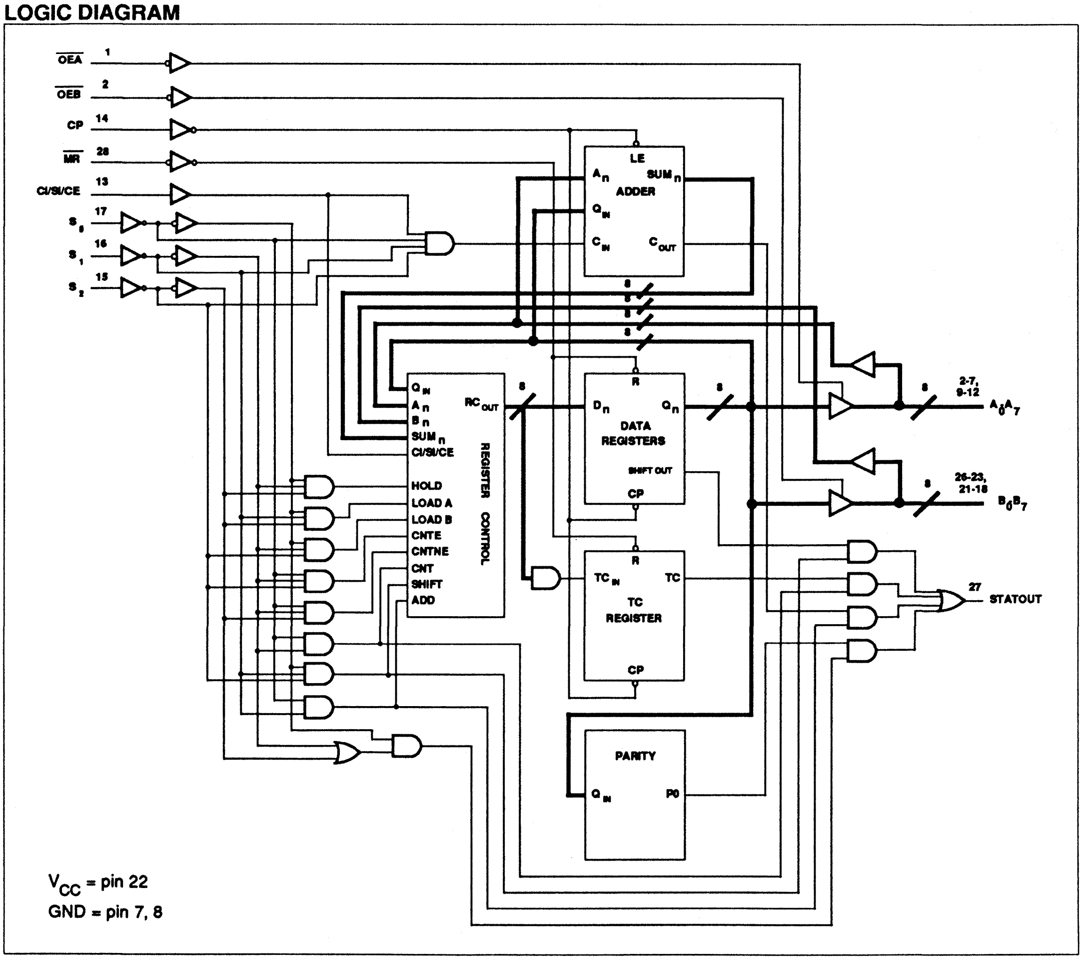
PLCC PIN CONFIGURATION



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS								INTERNAL REGISTER	DATA I/O		OUTPUT	OPERATING MODE
$\overline{MR}$	CP	$\overline{OE}_a$	$\overline{OE}_b$	S_0	S_1	S_2	CI/SI/CE	Q_n	A_n	B_n	STATOUT	
L	X	L	L	X	X	X	X	L	L	L	L	Clear
L	X	L	H	X	X	X	X	L	L	Z	L	
L	X	H	L	X	X	X	X	L	Z	L	L	
X	X	H	H	X	X	X	X	X	Z	Z	X	3-State
H	↑	X	L	L	L	L	CI/SI/CE	CI/SI/CE + a_{n0} + q_{n0}	a_{n1}	CI/SI/CE + a_{n0} + q_{n0}	C_{OUT}	Add Mode w/Carry In
H	↑	X	L	L	L	H	X	a_{n0}+ q_{n0}	a_{n1}	a_{n0} + q_{n0}	C_{OUT}	Add Mode wo/Carry In
H	↑	H	L	L	H	L	H	q_{n0} + 1	Z	q_{n0} + 1	TC(1)	Count w/Count Enable (count)
H	↑	L	H	L	H	L	H	q_{n0} + 1	q_{n0} + 1	Z	TC(1)	
H	↑	L	L	L	H	L	H	q_{n0} + 1	q_{n0} + 1	q_{n0} + 1	TC(1)	
H	X	H	L	L	H	L	L	q_{n0}	Z	q_{n0}	TC(1)	Count w/Count Enable (hold)
H	X	L	H	L	H	L	L	q_{n0}	q_{n0}	Z	TC(1)	
H	X	L	L	L	H	L	L	q_{n0}	q_{n0}	q_{n0}	TC(1)	
H	↑	H	L	L	H	H	X	q_{n0} + 1	Z	q_{n0} + 1	TC(1)	Count wo/Count Enable
H	↑	L	H	L	H	H	X	q_{n0} + 1	q_{n0} + 1	Z	TC(1)	
H	↑	L	L	L	H	H	X	q_{n0} + 1	q_{n0} + 1	q_{n0} + 1	TC(1)	
H	↑	H	L	H	L	L	CI/SI/CE	(3)	Z	(3)	Q_7	Shift
H	↑	L	H	H	L	L	CI/SI/CE	(3)	(3)	Z	Q_7	
H	↑	L	L	H	L	L	CI/SI/CE	(3)	(3)	(3)	Q_7	
H	↑	H	H	H	L	H	X	A_{n0}	a_{n0}	Z	Parity(2)	Load A Inputs
H	↑	H	L	H	L	H	X	A_{n0}	a_{n0}	A_{n0}	Parity(2)	
H	↑	L	X	H	L	H	X	Q_{n0}	q_{n0}	X	Parity(2)	
H	↑	H	H	H	H	L	X	B_{n0}	Z	b_{n0}	Parity(2)	Load B Inputs
H	↑	L	H	H	H	L	X	B_{n0}	B_{n0}	b_{n0}	Parity(2)	
H	↑	X	L	H	H	L	X	Q_{n0}	X	q_{n0}	Parity(2)	
H	X	L	H	H	H	H	X	Q_{n0}	Q_{n0}	Z	Parity(2)	Hold
H	X	H	L	H	H	H	X	Q_{n0}	Z	Q_{n0}	Parity(2)	
H	X	L	L	H	H	H	X	Q_{n0}	Q_{n0}	Q_{n0}	Parity(2)	

H = High voltage level.
L = Low voltage level.
a, b, q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition.
X = Don't care.
Z = High impedance.
↑ = Low-to-High clock transition.
(1) =Terminal count is High when the output is at terminal count (HHHHHHHH).
(2) = Parity is High for odd number of internal register bits High, Low for even number of internal register bits High.
(3) = CI/SI/CE→ Q_0→ Q_1, etc.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	μA
$I_{OZH}+I_{IH}$	Off state output current, High-level voltage applied	A_n, B_n	V_{CC} = MAX, V_O = 2.7V				70	μA
$I_{OZL}+I_{IL}$	Off state output current, Low-level voltage applied	A_n, B_n	V_{CC} = MAX, V_O = 0.5V				-70	μA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)					155	210	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Octal Shift/Count Transceiver FAST 74F807

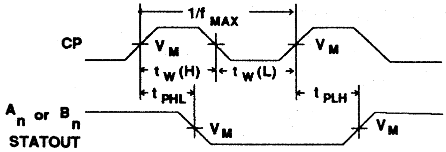
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to A_n or B_n(Load)	Waveform 1	9.0 5.0	10.5 6.5	11.5 9.5	8.0 4.5	13.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to A_n or B_n(Shift)	Waveform 1	9.0 4.5	10.5 6.5	12.5 9.5	8.0 4.5	15.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to A_n or B_n(Count)	Waveform 1	9.0 5.0	11.5 6.5	14.0 9.5	8.0 4.5	15.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to B_n(Add)	Waveform 1	9.0 5.0	10.5 6.5	11.5 9.5	8.0 4.5	13.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to STATOUT(Load A)	Waveform 1	17.5 12.5	19.5 14.5	22.5 17.0	15.5 11.5	26.5 19.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to STATOUT(Shift)	Waveform 1	11.0 7.0	13.0 8.5	15.5 11.5	9.5 6.5	18.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to STATOUT(Count)	Waveform 1	10.5 6.5	12.0 8.0	15.0 11.0	9.0 6.0	17.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to STATOUT(Add)	Waveform 1	13.0 8.5	15.0 10.5	18.0 13.0	11.5 8.0	20.5 14.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to A_n or B_n	Waveform 3	6.5	8.0	11.0	6.0	12.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to STATOUT(Load A)	Waveform 3	14.0	16.0	18.5	13.0	20.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to STATOUT(Shift)	Waveform 3	8.5	10.0	12.5	8.0	14.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to STATOUT(Count)	Waveform 3	8.5	10.0	12.5	8.0	14.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to STATOUT(Add)	Waveform 3	10.5	12.0	14.5	9.5	16.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to STATOUT(Add)	Waveform 4	6.5 8.0	14.0 14.0	23.5 22.5	5.5 7.5	26.5 27.0	ns
t_{PLH} t_{PHL}	Propagation delay CI/SI/CE to STATOUT	Waveform 4	19.5 21.0	21.5 22.5	24.0 25.5	17.0 20.0	28.0 29.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to STATOUT(Load A)	Waveform 4	8.0 7.5	10.0 11.5	12.5 15.5	7.0 7.0	14.5 17.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to STATOUT(Load B)	Waveform 4	6.5 8.0	10.0 12.0	13.0 15.0	5.5 7.0	15.0 16.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to STATOUT(Add)	Waveform 4	19.0 18.5	21.0 20.0	23.5 23.0	17.0 17.5	27.5 26.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to STATOUT(Shift)	Waveform 4	6.0 8.0	8.0 9.5	10.5 12.0	5.0 7.0	12.0 13.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEA}$ to A_n or $\overline{OEB}$ to B_n	Waveform 6 Waveform 7	2.5 4.0	4.5 5.5	7.0 8.5	2.0 3.5	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEA}$ to A_n or $\overline{OEB}$ to B_n	Waveform 6 Waveform 7	2.0 3.5	4.5 5.5	7.5 8.5	2.0 3.0	9.0 9.5	ns

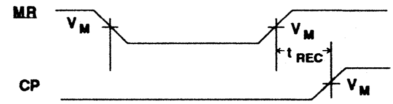
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n , B_n to CP (Load)	Waveform 5	6.0 9.5			6.5 12.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n , B_n to CP (Load)	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to CP (Add)	Waveform 5	10.5 16.5			12.0 21.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to CP (Add)	Waveform 5	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP(Add)	Waveform 5	16.0 16.0			20.0 18.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP (Count)	Waveform 5	16.5 19.5			19.0 22.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP (Shift)	Waveform 5	11.0 7.0			13.0 8.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP (Load)	Waveform 5	17.5 6.5			20.5 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP (All modes)	Waveform 5	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CI/SI/CE to CP (Add)	Waveform 5	10.0 18.0			11.5 22.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CI/SI/CE to CP (Count)	Waveform 5	8.5 16.0			10.0 18.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CI/SI/CE to CP (Shift)	Waveform 5	5.0 9.0			5.5 10.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CI/SI/CE to CP (All modes)	Waveform 5	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	5.5 4.5			6.0 4.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	4.5			5.0		ns
t_{REC}	Recovery Time, $\overline{MR}$ to CP	Waveform 2	2.0			2.0		ns

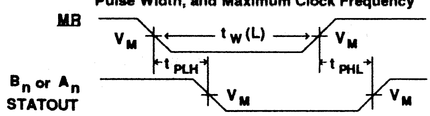
AC WAVEFORMS



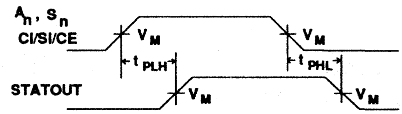
Waveform 1. Propagation Delay, Clock Input To Outputs, Clock Pulse Width, and Maximum Clock Frequency



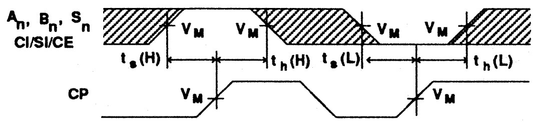
Waveform 2. Master Reset to Clock Recovery Time



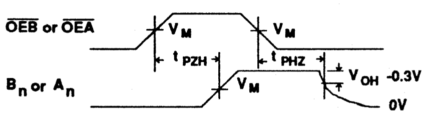
Waveform 3. Propagation Delay, Master Reset to Data or Master Reset to STATOUT



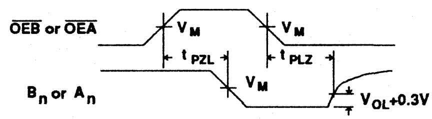
Waveform 4. Propagation Delay, Select to STATOUT, CI/SI/CE to STATOUT or Data to STATOUT



Waveform 5. Data Setup And Hold Times



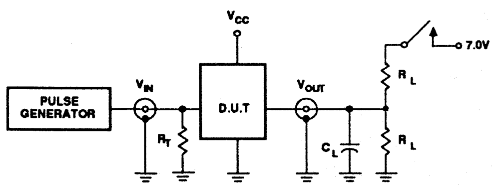
Waveform 6. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 7. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

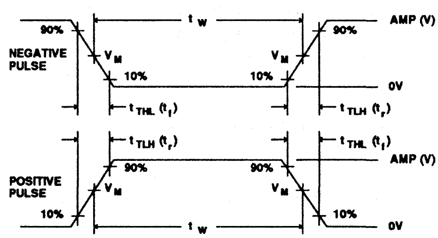
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-1304
ECN No.	99464
Date of issue	April 25, 1990
Status	Product Specification
FAST Products	

FAST 74F821/822/823/824/825/826

Bus Interface Registers

74F821/74F822 10-Bit Bus Interface Registers, NINV/INV (3-State)
74F823/74F824 9-Bit Bus Interface Registers, NINV/INV (3-State)
74F825/74F826 8-Bit Bus Interface Registers, NINV/INV (3-State)

FEATURES

- **High speed parallel registers with positive edge-triggered D-type flip-flops**
- **High performance bus interface buffering for wide data/address paths or busses carrying parity**
- **High impedance PNP base inputs for reduced loading (20µA in High and Low states)**
- **I_{IL} is 20µA vs 1000µA for AM29821 series**
- **Buffered control inputs to reduce AC effects**
- **Ideal where high speed, light loading, or increased fan-in as required with MOS microprocessors**
- **Positive and negative over-shoots are clamped to ground**
- **3-state outputs glitch free during power-up and power-down**
- **Slim Dip 300 mil package**
- **Broadside pinout compatible with AMD AM 29821-29826 series**
- **Outputs sink 64mA and source 24mA**

DESCRIPTION

The 74F821 series Bus Interface Registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of busses carrying parity.

The 'F821/'F822 are buffered 10-bit wide versions of the popular 'F374/'F534 functions.
The 'F822 is the inverted output version of 'F821.

The74F823 and 74F824 are 9-bit wide

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F821, 74F822	180MHz	75mA
74F823, 74F824	180MHz	70mA
74F825, 74F826	180MHz	65mA

ORDERING INFORMATION

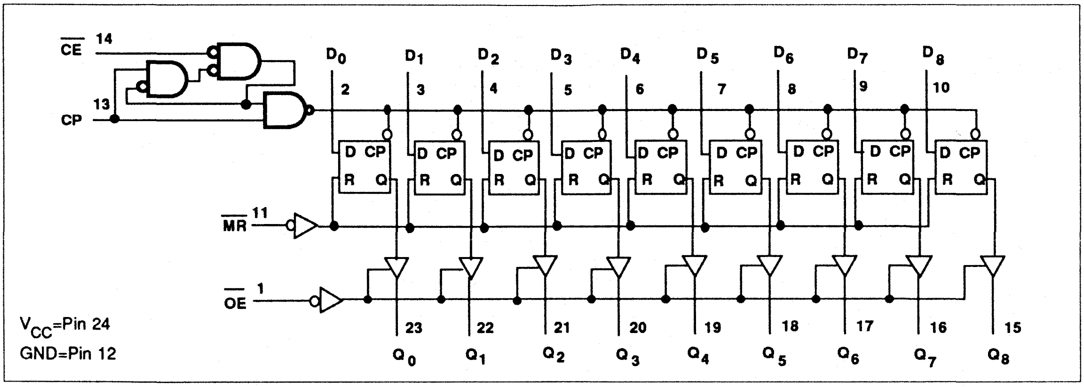
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic SLIM DIP (300mil)	N74F821N, N74F822N, N74F823N, N74F824N, N74F825N, N74F826N
24-Pin Plastic SOL	N74F821D, N74F822D, N74F823D, N74F824D, N74F825D, N74F826D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

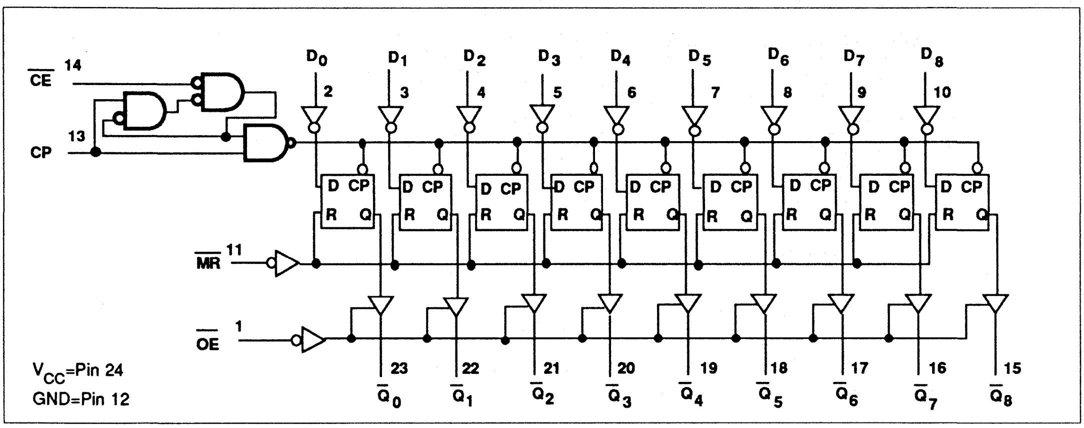
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F821 'F822	D_n	Data inputs	1.0/0.033	20µA/20µA
	CP	Clock input	1.0/0.033	20µA/20µA
	$\overline{OE}$	Output enable input (activeLow)	1.0/0.033	20µA/20µA
	Q_n, $\overline{Q}_n$	Data output	1200/106.7	24mA/64mA
'F823 'F824	D_n	Data inputs	1.0/0.033	20µA/20µA
	CP	Clock input	1.0/0.033	20µA/20µA
	$\overline{CE}$	Clock enable input (active Low)	1.0/0.033	20µA/20µA
	$\overline{MR}$	Master reset input (active Low)	1.0/0.033	20µA/20µA
	$\overline{OE}$	Output enable input (active Low)	1.0/0.033	20µA/20µA
	Q_n, $\overline{Q}_n$	Data outputs	1200/106.7	24mA/64mA
'F825 'F826	D_n	Data inputs	1.0/0.033	20µA/20µA
	CP	Clock input	1.0/0.033	20µA/20µA
	$\overline{CE}$	Clock enable input (active Low)	1.0/0.033	20µA/20µA
	$\overline{MR}$	Master reset input (active Low)	1.0/0.033	20µA/20µA
	$\overline{OE}_n$	Output enable inputs (active Low)	1.0/0.033	20µA/20µA
	Q_n, $\overline{Q}_n$	Data outputs	1200/106.7	24mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC DIAGRAM for 'F823



LOGIC DIAGRAM for 'F824



FUNCTION TABLE for 'F823 and 'F824

INPUTS					OUTPUTS		OPERATING MODE
					'F823	'F824	
$\overline{OE}$	$\overline{MR}$	$\overline{CE}$*	CP	D_n	Q	$\overline{Q}$	
L	L	X	X	X	L	L	Clear
L	H	L	↑	h	H	L	Load and read data
L	H	L	↑	l	L	H	
L	H	H	X	X	NC	NC	Hold
H	X	X	X	X	Z	Z	High impedance

H = High voltage level
L = Low voltage level
h = High state must be present one setup time before the Low-to-High clock transition
l = Low state must be present one setup time before the Low-to -High clock transition
↑ = Low-to-High clock transition
X = Don't care
NC = No change
Z = High impedance "off" state

* = Since $\overline{CE}$ input is sensitive to very short (<3ns) High-to-Low-to-High going spikes while CP is High, users should avoid the use of decoders or other potentially glitch prone devices on the $\overline{CE}$ input.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} =-15mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.4			V
		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} =-24mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=64mA	±10%V_{CC}			0.55	V
				±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					-20	μA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	μA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V					-50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	'F821 'F822	I_{CCH}	V_{CC} = MAX		75	105	mA
			I_{CCL}			75	105	mA
			I_{CCZ}			75	115	mA
		'F823 'F824	I_{CCH}	V_{CC} = MAX		65	100	mA
			I_{CCL}			70	105	mA
			I_{CCZ}			75	110	mA
		'F825 'F826	I_{CCH}	V_{CC} = MAX		60	85	mA
			I_{CCL}			60	90	mA
			I_{CCZ}			65	95	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	Maximum clock frequency PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	150	180		140		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	'F821,'F823 'F825,'F826	Waveform 1	4.0 4.0	6.5 6.0	8.5 8.5	4.0 3.5	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$	'F822 'F824	Waveform 1	4.5 4.5	6.5 6.5	9.0 9.0	4.5 4.5	10.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n or $\overline{Q}_n$	'F823, 'F824 'F825, 'F826	Waveform 2	3.0	5.0	8.0	3.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable time OE_n to Q_n or $\overline{Q}_n$		Waveform 4 Waveform 5	5.0 3.0	7.0 5.0	10.0 8.0	4.0 2.5	11.5 9.0	ns
t_{PHZ} t_{PLZ}	Propagation delay OE_n to Q_n or $\overline{Q}_n$		Waveform 4 Waveform 5	1.5 1.5	3.5 3.5	6.5 6.5	1.5 1.5	7.5 7.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 3	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 3	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	3.5 3.5			4.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	'F823 'F824 'F825 'F826	Waveform 3	0.0 2.0			0.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		Waveform 3	0.0 3.0			0.0 3.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low		Waveform 2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP		Waveform 2	2.5			2.5		ns

Document No.	853-0615
ECN No.	99490
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F835
Shift Register

8-Bit Shift Register with 2:1 Mux-In, Latched "B" Inputs, and Serial Out

FEATURES
- **Specifically designed for Video applications**
- **Combines the 'F373, two 'F157s, and the 'F166 functions in one package**
- **Interleaved loading with 2:1 mux**
- **Dual 8-bit Parallel Inputs**
- **Transparent Latch on all "B" Inputs**
- **Guaranteed Serial Shift Frequency to 100MHz**
- **Expandable to 16-bits or more with serial input**

DESCRIPTION

The 74F835 is a high speed 8-bit parallel/serial-in, serial-out shift register whose parallel inputs have been connected to an internal octal two-to-one multiplexer with all the 'B' inputs connected to an octal latch.

This 24 pin part is specifically designed for video bit shifting, where interleaved loading is desired and parts count is critical. However, and it is useful in any design where a 2:1 mux input with a transparent latch is needed.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F835	150MHz	45mA

ORDERING INFORMATION

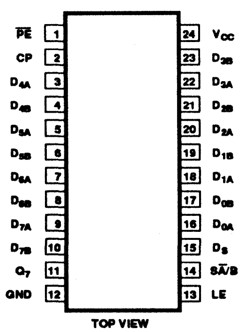
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F835N
24-Pin Plastic SOL	N74F835D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

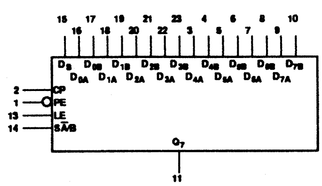
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{0A} - D_{7A}	Parallel data inputs	1.0/1.0	20μA/0.6mA
D_{0B} - D_{7B}	Latched Parallel data inputs	1.0/1.0	20μA/0.6mA
D_S	Serial data input	1.0/1.0	20μA/0.6mA
CP	Shift Register Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
$S\overline{A}/B$	Mux Select	1.0/1.0	20μA/0.6mA
LE	Latch Enable input (for B inputs)	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel Enable input	1.0/1.0	20μA/0.6mA
Q_7	Output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

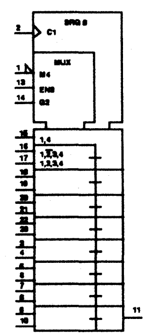


LOGIC SYMBOL



V_{CC} = pin 24
GND = pin 12

LOGIC SYMBOL(IEEE/IEC)



DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximun input voltage	V_{CC} =MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} =MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} =MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} =MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} =MAX			45	65	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

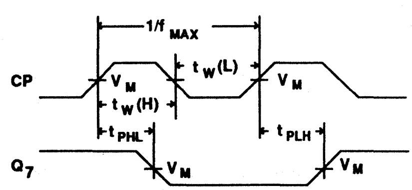
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	130	150		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_7 (Load)	Waveform 1	5.0 5.0	7.0 7.0	9.5 9.5	5.0 5.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_7 (Shift)	Waveform 1	5.0 5.0	7.0 7.0	9.5 9.5	5.0 5.0	10.0 10.0	ns

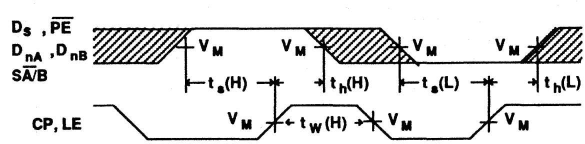
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Typ	Max	LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$ Min	Max	UNIT
$t_s(H)$ $t_s(L)$	Setup time D_{nA} or D_{nB} to CP	Waveform 2	3.5 3.5			3.5 3.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_{nA} or D_{nB} to CP	Waveform 2	1.0 1.0			1.5 1.5		ns
$t_s(H)$ $t_s(L)$	Setup time D_S to CP	Waveform 2	1.0 1.0			1.5 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_S to CP	Waveform 2	2.0 2.0			2.5 2.5		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{PE}$ to CP	Waveform 2	3.5 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{PE}$ to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time D_{nB} to LE	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_{nB} to LE	Waveform 2	3.0 3.0			4.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time $S\overline{A}/B$ to CP	Waveform 2	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time $S\overline{A}/B$ to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width, High or Low	Waveform 1	4.5 4.5			5.5 5.0		ns
$t_w(H)$	Latch Enable pulse width, High	Waveform 1	4.5			5.0		ns

AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data and Select Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Document No.	853-1208
ECN No.	99396
Date of issue	April 18, 1990
Status	Product Specification
FAST Products	

FAST 74F841/842/843/844/845/846

Bus Interface Latches

'F841/'F842 10-Bit Bus Interface Latches, NINV/INV (3-State)
'F843/'F844 9-Bit Bus Interface Latches, NINV/INV (3-State)
'F845/'F846 8-Bit Bus Interface Latches, NINV/INV (3-State)

FEATURES

- **High speed parallel latches**
- **Extra data width for wide address/data paths or busses carrying parity**
- **High impedance NPN base input structure minimizes bus loading**
- **I_{IL} is 20µA vs 1000µA for AM29841 series**
- **Buffered control inputs to reduce AC effects**
- **Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors**
- **Positive and negative over-shoots are clamped to ground**
- **3-state outputs glitch free during power-up and power-down**
- **48mA sink current**
- **Slim Dip 300 mil package**
- **Broadside pinout**
- **Pin-for-pin and function compatible with AMD AM29841-846 series**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F841, 74F842	5.5ns	60mA
74F843, 74F845	5.5ns	75mA
74F844, 74F846	6.2ns	60mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V\pm10\%$; $T_A = 0°C$ to $+70°C$
24-Pin Plastic Slim DIP (300mil)	N74F841N, N74F842N, N74F843N, N74F844N, N74F845N, N74F846N
24-Pin Plastic SOL	N74F841D, N74F842D, N74F843D, N74F844D, N74F845D, N74F846D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data inputs	1.0/0.033	20µA/20µA
LE	Latch Enable input	1.0/0.033	20µA/20µA
$\overline{OE}$, $\overline{OE}_n$	Output Enable input (active-Low)	1.0/0.033	20µA/20µA
$\overline{MR}$	Master Reset input (active-Low)	1.0/0.033	20µA/20µA
$\overline{PRE}$	Preset input (active-Low)	1.0/0.033	20µA/20µA
Q_n	Data outputs	1200/80	24mA/48mA
$\overline{Q}_n$	Data outputs	1200/80	24mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 'F841-'846 bus interface latch series are designed to provide extra data width for wider address/data paths of busses carrying parity.

The 'F841-'F846 series are functionally and pin compatible to the AMD AM29841-AM29846 series.

The 'F841 consists of ten D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High the output is in the High-impedance state.

The 'F842 is the inverted output version of 'F841.

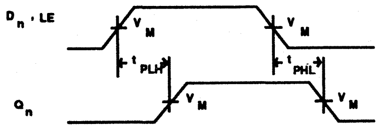
The 'F843 consists of nine D-type latches with 3-state outputs. In addition to the LE and $\overline{OE}$ pins, the 'F843 has a Master Reset ($\overline{MR}$) pin and Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{MR}$ is Low, the outputs are Low if $\overline{OE}$ is Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are High, if $\overline{OE}$ is Low. $\overline{PRE}$ overrides $\overline{MR}$.

The 'F844 is the inverted output version of 'F843.

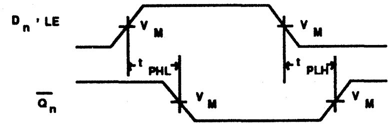
The 'F845 consists of eight D-type latches with 3-state outputs. In addition to the LE, $\overline{OE}$, $\overline{MR}$ and $\overline{PRE}$ pins, the 'F845 has two additional $\overline{OE}$ pins making a total of three Output Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) pins. The multiple Output Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$.

The 'F846 is the inverted output version of 'F845.

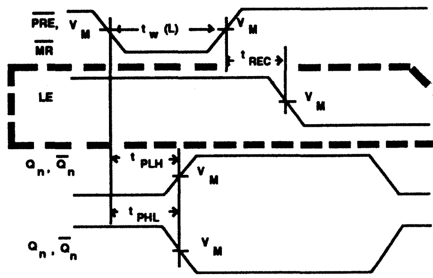
AC WAVEFORMS



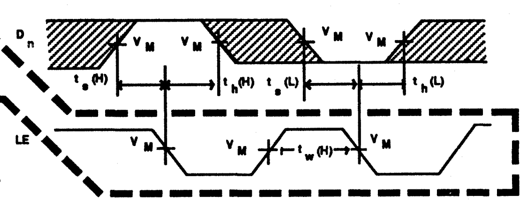
Waveform 1. Propagation Delay, Non-Inverting Path



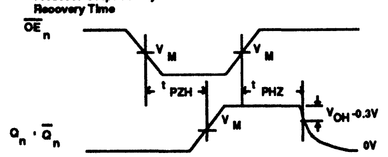
Waveform 2. Propagation Delay, Inverting Path



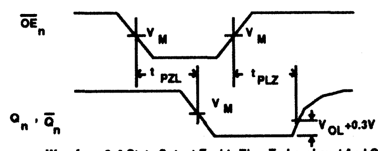
Waveform 3. Master Reset and Preset Pulse Width, Master Reset and Preset to Output Delay and Master Reset and Preset to Latch Enable Recovery Time



Waveform 4. Data Setup And Hold Times



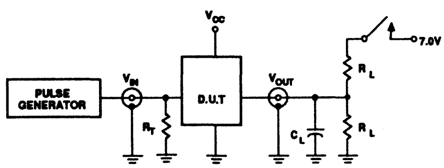
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



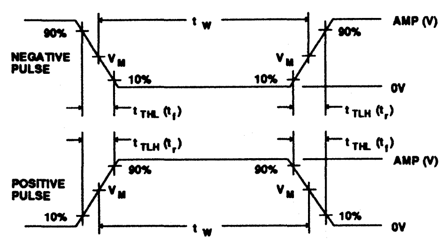
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F1604
LATCH

Document No.	853-0088
ECN No.	97744
Date of issue	September 27, 1989
Status	Product Specification
FAST Products	

Dual Octal Latch

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1604	7.0 ns	70mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20µA in High and Low state)**
- **Stores 16-Bit-Wide data inputs, multiplexed 8-Bit outputs**
- **Propagation delay 7.0ns typical**
- **Power supply current 70mA typical**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F1604N
28-Pin Plastic SOL	N74F1604D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

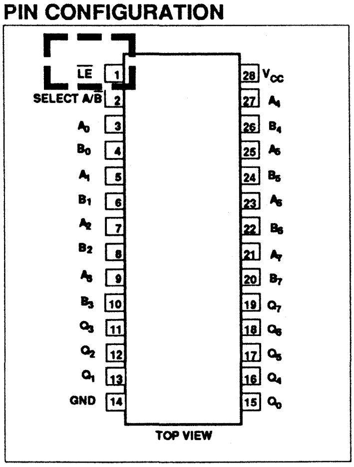
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_n, B_n	Data inputs	1.0/.033	20µA/20µA
SELECT $A/\overline{B}$	Select input	1.0/.033	20µA/20µA
$\overline{LE}$	Latch Enable input (Active Low)	1.0/.033	20µA/20µA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

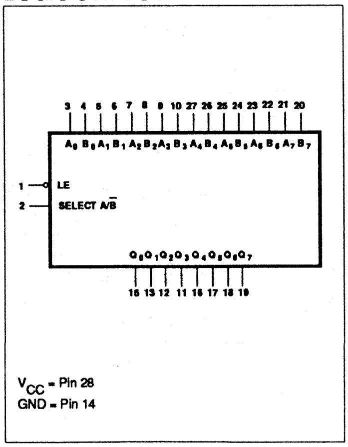
DESCRIPTION

The 74F1604 is a Dual Octal Transparent Latch. Organized as 8-bit A and B latches, the latch outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT $A/\overline{B}$) input determines whether the A or B latch contents are multiplexed to the eight outputs. Data from the B inputs are selected when SELECT $A/\overline{B}$ is Low: data from the A inputs are selected when SELECT $A/\overline{B}$ is High. Data enters the latch on the falling edge of the Latch Enable ($\overline{LE}$) input. The Latch remains transparent to the data inputs while $\overline{LE}$ is Low, and stores the data that is present one setup time before the Low-to-High Latch Enable transition

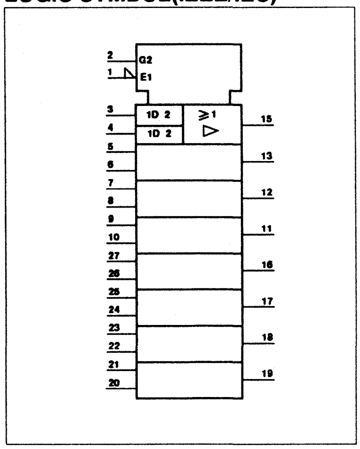
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Document No.	
ECN No.	
Date of issue	August 23, 1989
Status	Preliminary Specification
FAST Products	

FAST 74F1760
4-Way Latched Address Multiplexer

FEATURES

- **Consists of 10 bit wide 4-1 multiplexer**
- **Separate address latch input for each channel**
- **3-state address outputs**
- **Designed for address multiplexing of dynamic RAMs and other applications**

TYPE	TYPICAL PRPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1760	5.5ns	55 mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A=0°C to 70°C
64-Pin Plastic DIP	74F1760N
68-Pin PLCC	74F1760A

PRODUCT DESCRIPTION

The 'F1760 is a 10 bit wide 4-1 multiplexer. Each 10-bit channel has a separate address latch enable pin thus eliminating the need for external address latches. The 'F1760 has a common pair of Select (SEL_0, SEL_1) inputs to select between channels and a common Output Enable ($\overline{OE}$) pin to control the 3-State outputs.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

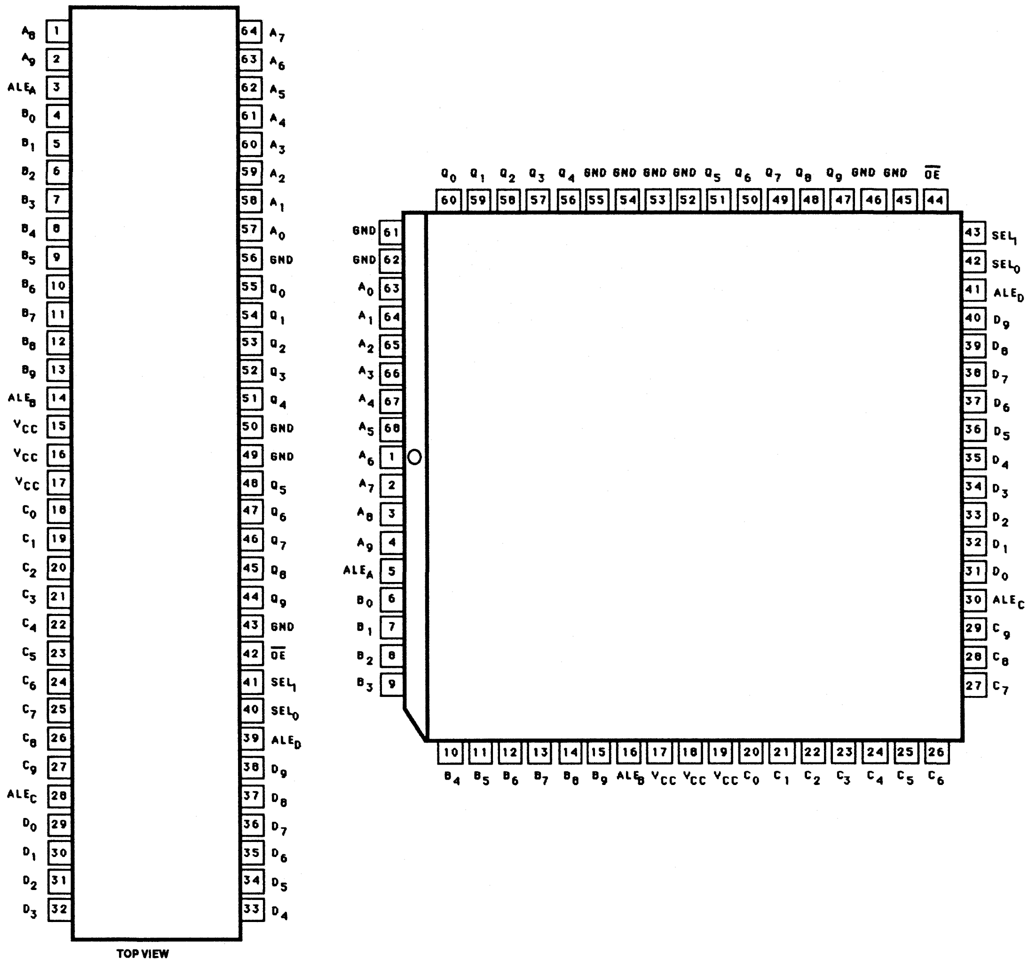
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_9	Address Inputs	1.0/1.0	20 µA/0.6 mA
B_0-B_9	Address Inputs	1.0/1.0	20 µA/0.6 mA
C_0-C_9	Address Inputs	1.0/1.0	20 µA/0.6 mA
D_0-D_9	Address Inputs	1.0/1.0	20 µA/0.6 mA
SEL_0-SEL_1	Select Inputs	1.0/1.0	20 µA/0.6 mA
ALE_A	Address Latch Enable input	1.0/1.0	20 µA/0.6 mA
ALE_B	Address Latch Enable input	1.0/1.0	20 µA/0.6 mA
ALE_C	Address Latch Enable input	1.0/1.0	20 µA/0.6 mA
ALE_D	Address Latch Enable input	1.0/1.0	20 µA/0.6 mA
$\overline{OE}$	Output Enable input	1.0/1.0	20 µA/0.6 mA
Q_0-Q_9	Address Outputs	N/A	15 mA/24 mA

NOTE:
One (1.0) FAST Unit Load is defined as 20 uA in the HIGH state and 0.6 mA in the LOW state.

4-Way Latched Address Multiplexer

FAST 74F1760

PIN CONFIGURATION



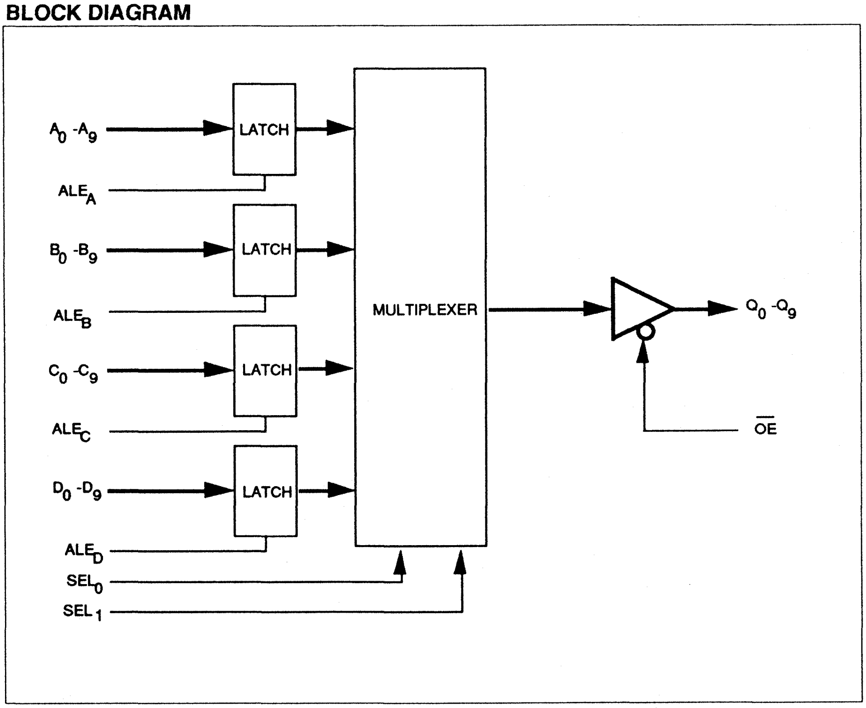
4-Way Latched Address Multiplexer

FAST 74F1760

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A_0-A_9	57-64, 1-2	63-68, 1-4	Inputs	Address inputs
B_0-B_9	4-13	6-15	Inputs	Address inputs
C_0-C_9	18-27	20-29	Inputs	Address inputs
D_0-D_9	29-38	31-40	Inputs	Address inputs
ALE_A	3	5	Input	Address Latch Enable for A_0-A_9
ALE_B	14	16	Input	Address Latch Enable for B_0-B_9
ALE_C	28	30	Input	Address Latch Enable for C_0-C_9
ALE_D	39	41	Input	Address Latch Enable for D_0-D_9
SEL_0	40	42	Input	Select input
SEL_1	41	43	Input	Select input
$\overline{OE}$	42	44	Input	Output Enable input
Q_9-Q_0	44-48, 51-55	47-51, 56-60	Outputs	Address outputs

BLOCK DIAGRAM



4-Way Latched Address Multiplexer

FAST 74F1760

FUNCTION TABLE

A_0-A_9	ALE_A	B_0-B_9	ALE_B	C_0-C_9	ALE_C	D_0-D_9	ALE_D	SEL_0	SEL_1	Q_0-Q_9	$\overline{OE}$	COMMENTS
XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	Hi-Z	High	Outputs 3-stated
a_0-a_9	↓	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	A-inputs latched into latch A
a_0-a_9	Note	XX	XX	XX	XX	XX	XX	Low	Low	a_0-a_9	Low	a_0-a_9 appear on Y_0-Y_9 outputs
XX	XX	b_0-b_9	↓	XX	XX	XX	XX	XX	XX	XX	XX	B-inputs latched into latch B
XX	XX	b_0-b_9	Note	XX	XX	XX	XX	High	Low	b_0-b_9	Low	b_0-b_9 appear on Y_0-Y_9 outputs
XX	XX	XX	XX	c_0-c_9	↓	XX	XX	XX	XX	XX	XX	C-inputs latched into latch C
XX	XX	XX	XX	c_0-c_9	Note	XX	XX	Low	High	c_0-c_9	Low	c_0-c_9 appear on Y_0-Y_9 outputs
XX	XX	XX	XX	XX	XX	d_0-d_9	↓	XX	XX	XX	XX	D-inputs latched into latch A
XX	XX	XX	XX	XX	XX	d_0-d_9	Note	High	High	d_0-d_9	Low	d_0-d_9 appear on Y_0-Y_9 outputs

NOTE:
ALE_n may be High (transparent mode) or Low (if data has been latched previously by a High to Low transition on ALE_n.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current[1]			-15	mA
I_{OL}	Low-level output current[1]			24	mA
T_A	Operating free-air temperature range	0		70	°C

NOTE:
1. Transcient currents will exceed these values in actual operation

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH2}[3] = -35mA	±10%V_{CC}	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
			I_{OL2}[4] = 60mA	±10%V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage	V_{CC}= MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short circuit output current[5]	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	V_{CC}= MAX				55	75	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH2} is the current necessary to guarantee a Low to High transition in a 70Ω transmission line.
4. I_{OL2} is the current necessary to guarantee a High to Low transition in a 70Ω transmission line.
5. Not more than one output should be shorted at a time. For testing I_{os}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.

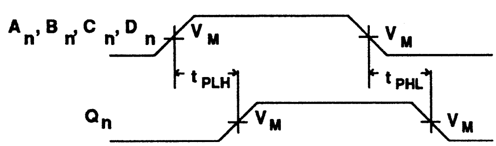
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 300pF$, $R_L = 70\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm10\%$, $C_L = 300pF$, $R_L = 70\Omega$		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n, C_n, D_n to Q_n	Waveform 1	4.0 4.0	4.5 4.5	8.0 8.0	4.0 4.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay SEL_n to Q_n	Waveform 2	4.0 4.0	5.5 4.5	8.0 8.0	4.0 4.0	7.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	Waveform 4 Waveform 5	2.0 4.0	3.0 5.0	4.0 7.0	2.0 4.0	4.0 7.0	ns
t_{PZH} t_{PZL}	Output Disable time $\overline{OE}$ to Q_n	Waveform 4 Waveform 5	2.0 2.0	3.0 3.5	4.0 5.5	2.0 2.0	4.0 5.5	ns

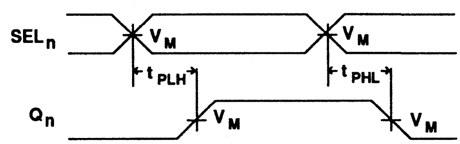
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 300pF$, $R_L = 70\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm10\%$, $C_L = 300pF$, $R_L = 70\Omega$		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n, B_n, C_n, D_n to ALE_n	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n, B_n, C_n, D_n to ALE_n	Waveform 3	2.0 2.0			2.0 2.0		ns

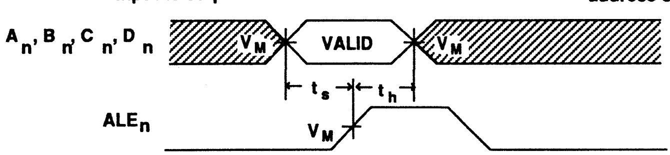
AC WAVEFORMS



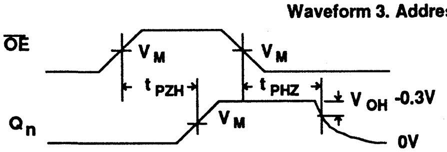
Waveform 1. Propagation Delay, Address input to output



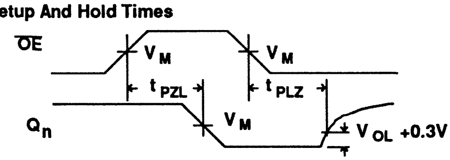
Waveform 2.Propagation Delay, SEL_n inputs to address outputs



Waveform 3. Address Setup And Hold Times



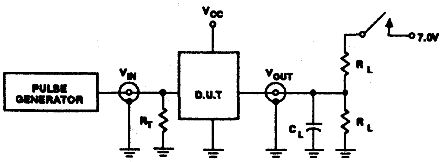
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

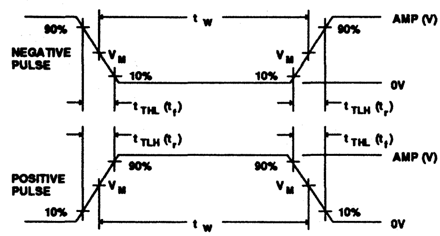
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F1763
Intelligent DRAM Controller (IDC)

FAST Products

Product Specification

TYPE	f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1763	100 MHz	150 mA

FEATURES

- **DRAM signal timing generator**
- **Automatic refresh circuitry**
- **Selectable row address hold and $\overline{RAS}$ precharge times**
- **Facilitates page mode accesses**
- **Controls 1 MBit DRAMs**
- **Intelligent burst-mode refresh after page-mode access cycles**

PRODUCT DESCRIPTION

The Philips Intelligent Dynamic RAM Controller is a 1 MBit, single-port version of the 74F764 Dual Port Dynamic RAM Controller. It contains automatic signal timing, address multiplexing and refresh control required for interfacing with dynamic RAMs. Additional features have been added to this device to take advantage of technological advances in Dynamic RAMs. A Page-Mode access pin allows the user to assert $\overline{RAS}$ for the entire access cycle rather than the predefined four-clock-cycle pulse width used for normal random access cycles. In addition, the user has the ability to select the $\overline{RAS}$ precharge time and Row-Address Hold time to fit the particular DRAMs being used. $\overline{DTACK}$ has been modified from previous family parts to become a negative true, tri-stated output. The options for latched or unlatched address are contained on a single device by the addition of an Address Latch Enable ($\overline{ALE}$) input. Finally, a burst refresh monitor has been added to ensure complete refreshing after lengthy page-mode access cycles. With a maximum clock frequency of 100 MHz, the F1763 is capable of controlling DRAM arrays with access times down to 40 nsec.

ORDERING INFORMATION

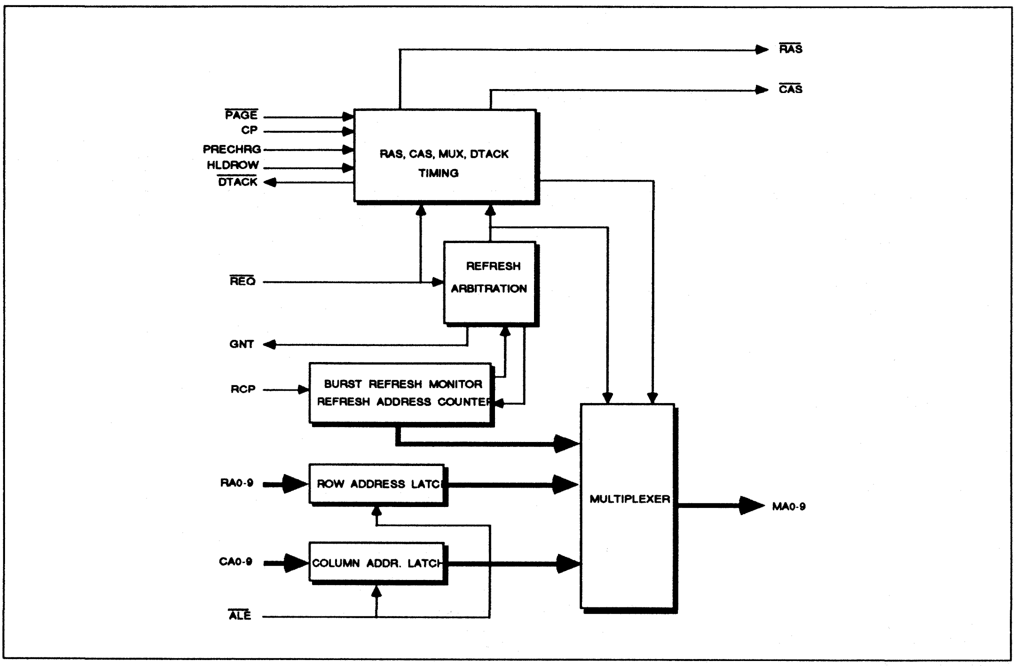
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A=0°C to 70°C
48-Pin Plastic DIP	N74F1763N
44-Pin PLCC	N74F1763A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

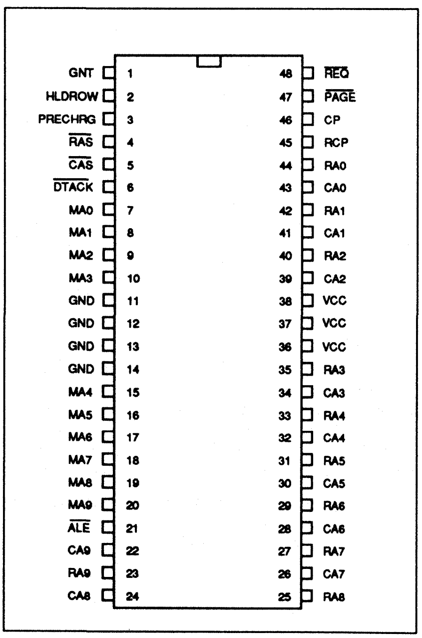
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{REQ}$	DRAM Request Input	1.0/1.0	20 µA/0.6 mA
CP	Clock Input	1.0/1.0	20 A/0.6 mA
$\overline{PAGE}$	Page Mode Select Input	1.0/1.0	20 A/0.6 mA
PRECHRG	$\overline{RAS}$ Precharge Select Input	1.0/1.0	20 A/0.6 mA
HLDROW	Row Hold Select Input	1.0/1.0	20 A/0.6 mA
$\overline{DTACK}$	Data Transfer Ack. Output	50/80	35 mA/60 mA
GNT	Access Grant Output	50/80	35 mA/60 mA
RCP	Refresh Clock Input	1.0/1.0	20 A/0.6 mA
RA0-9	Row Address Inputs	1.0/1.0	20 A/0.6 mA
CA0-9	Column Address Inputs	1.0/1.0	20 A/0.6 mA
$\overline{ALE}$	Address Latch Enable Input	1.0/1.0	20 A/0.6 mA
$\overline{RAS}$	Row Address Strobe Output	N/A*	35 mA/60 mA
$\overline{CAS}$	Column Address Strobe Output	N/A*	35 mA/60 mA
MA0-9	DRAM Address Outputs	N/A*	35 mA/60 mA

NOTE:
One (1.0) FAST Unit Load is defined as 20 uA in the HIGH state and 0.6 mA in the LOW state.
* FAST Unit Loads do not correspond to DRAM Input Loads. See Functional Description for details.

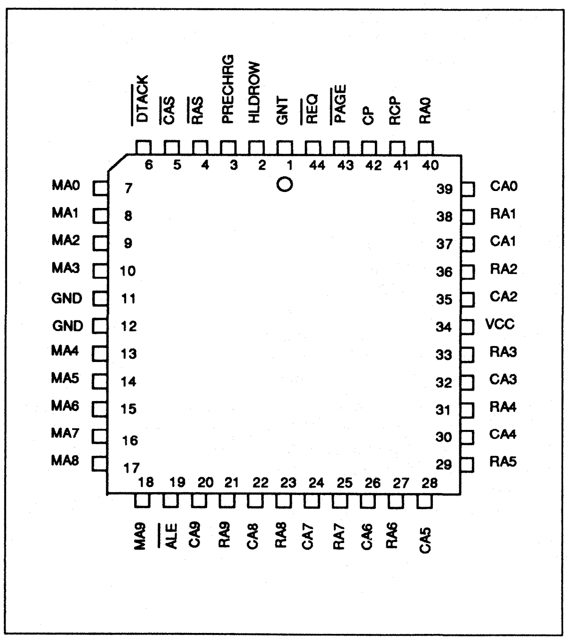
BLOCK DIAGRAM



DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
$\overline{REQ}$	48	44	Input	Active Low Memory Access Request input, must be asserted for the entire DRAM access cycle. $\overline{REQ}$ is sampled on the rising edge of the CP clock.
GNT	1	1	Input	Active High Grant output. When High indicates that a DRAM access (inactive during refresh) cycle has begun. Asserted from the rising edge of the CP clock.
$\overline{PAGE}$	47	43	Input	Active Low Page-Mode Access input. Forces the IDC to keep $\overline{RAS}$ asserted for as long as the $\overline{PAGE}$ input is Low and $\overline{REQ}$ is asserted Low.
HLDROW	2	2	Input	Row Address Hold input. If Low will configure the IDC to maintain the row addresses for a full CP clock cycle after $\overline{RAS}$ is asserted. If High will program the IDC to maintain row addresses for a 1/2 CP clock cycle after $\overline{RAS}$ is asserted.
PRECHRG	3	3	Input	$\overline{RAS}$ Precharge input. A Low will program the IDC to guarantee a minimum of 4 CP clock cycles of precharge. A High will guarantee 3 clock cycles of precharge.
CP	46	42	Input	Clock input. Used by the Controller for all timing and arbitration functions.
RCP	45	41	Input	Refresh Clock input. Divided internally by 64 to produce an internal Refresh Request.
$\overline{DTACK}$	6	6	Output	Active Low, 3-state Data Transfer Acknowledge output. Enabled by the $\overline{REQ}$ input and asserted four clock cycles after the assertion of $\overline{RAS}$. 3-stated when $\overline{REQ}$ goes High.
RA0-9	44,42, 40,35, 33,31, 29,27, 25,23	40, 38, 36, 33, 31, 29, 27, 25, 23, 21	Inputs	Row Address inputs.
CA0-9	43,41, 39,34, 32,30, 28,26, 24,22	39, 37, 35, 32, 30, 28, 26, 24, 22, 20	Inputs	Column Address inputs. Propagated to the MA0-9 outputs 1 CP clock cycle after $\overline{RAS}$ is asserted, if HLDROW=0 or 1/2 clock cycle later if HLDROW is 1.
$\overline{RAS}$	4	4	Output	Active Low Row Address Strobe. Asserted for four clock cycles during each refresh cycle regardless of the $\overline{PAGE}$ input. Also asserted for four clock cycles during processor access if the $\overline{PAGE}$ input is High. If $\overline{PAGE}$ is Low, $\overline{RAS}$ is negated upon negation of $\overline{PAGE}$ or $\overline{REQ}$, whichever occurs first.
$\overline{CAS}$	5	5	Output	Active Low Column Address Strobe. Always asserted 1.5 CP clock cycles after the assertion of $\overline{RAS}$. Negated upon negation of $\overline{REQ}$. HLDROW input pin does not affect $\overline{RAS}$ to $\overline{CAS}$ timing.
MA0-9	7-10, 15-20	7-10, 13-18	Output	DRAM multiplexed address outputs. Row and column addresses asserted on these pins during an access cycle. Refresh counter addresses presented on these outputs during refresh cycles.
$\overline{ALE}$	21	19	Input	Active Low Address Latch Enable input. A Low on this pin will cause the address latches to be transparent. A High level will latch the RA0-9 & CA0-9 inputs.
V_{CC}	36-38	34		+5 V ± 10% Supply voltage.
GND	11-14	11, 12		Ground

FUNCTIONAL DESCRIPTION

The 74F1763 1 Megabit Intelligent DRAM Controller (IDC) is a synchronous device with most signal timing being a function of the CP input clock.

Arbitration:

Once the DRAM's $\overline{RAS}$ precharge time has been satisfied, the $\overline{REQ}$ input is sampled on each rising edge of the CP clock and an internally generated refresh request is sampled on each falling edge of the same clock. When only one of these requests is sampled as active the appropriate memory cycle will begin immediately. For a memory access cycle this will be indicated by GNT and $\overline{RAS}$ outputs both being asserted and for a refresh cycle by multiplexing refresh address to the MA0-9 outputs and subsequent assertion of $\overline{RAS}$ after 1/2CP clock cycle. If both memory access and refresh requests are active at a given time the request sampled first will begin immediately and the other request (if still asserted) will be serviced upon completion of the current cycle and it's associated $\overline{RAS}$ precharge time.

Memory access:

The row (RA0-9) and column (CA0-9) address inputs are latched when $\overline{ALE}$ input is High. When $\overline{ALE}$ is Low the input addresses propagate directly to the outputs. When GNT and RAS are asserted , after a $\overline{REQ}$ has been sampled the RA0-9 address inputs will have already propagated to the MA0-9 outputs for the row address. One or one-half CP clock cycles later (depending on the state of the HLDROW input) the column address (CA0-9) inputs are propagated to the MA0-9 outputs. $\overline{CAS}$ is always asserted one and one-half CP clock cycles after $\overline{RAS}$ is asserted. If the $\overline{PAGE}$ input is High, $\overline{RAS}$ will be negated approximately four CP clock cycles after its initial assertion. At this time the $\overline{DTACK}$ output becomes valid indicating the completion of a memory access cycle. The IDC will maintain the state of all its outputs untill the $\overline{REQ}$ input is negated (see timing waveforms).

Row address hold times:

If the HLDROW input of the IDC is High the row address outputs will remain valid 1/2 CP clock cycle after $\overline{RAS}$ is asserted. If the HLDROW input is Low the row address outputs will remain valid one CP clock cycle after $\overline{RAS}$ is asserted.

$\overline{RAS}$ precharge timing:

In order to meet the $\overline{RAS}$ precharge requirement of dynamic RAMs, the controller will hold-off a subsequent $\overline{RAS}$ signal assertion due to a processor access request or a refresh cycle for four or three full CP clock cycles from the previous negation of $\overline{RAS}$, depending on the state of the PRECHRG input. If the PRECHRG input is Low, $\overline{RAS}$ remains High for at least 4 CP clock cycles. If the PRECHRG input is High $\overline{RAS}$ remains High for at least 3 CP clock cycles.

Refresh timing:

The refresh address counter wakes-up in an all 1's state and is an up counter. The refresh clock (RCP) is internally divided down by 64 to produce an internal refresh request. This refresh request is recognized either immediately or at the end of a running memory access cycle. Due to the possibility that page mode access cycles may be lengthy, the controller keeps track of how many refresh requests have been missed by logging them internally (up to 128) and servicing any pending refresh requests at the end of the memory access cycle. The controller performs $\overline{RAS}$-only refresh cycles until all pending refresh requests are depleted.

Page-mode access:

Fast accesses to consecutive locations of DRAM can be realized by asserting the $\overline{PAGE}$ input as shown in the timing waveforms. In this mode, the controller does not automatically negate $\overline{RAS}$ after four CP clock cycles, but keeps it asserted throughout the access cycle. By using external gates, the $\overline{CAS}$ output can be gated on and off while changing the column address inputs to the controller, which will propogate to the MA_0 - MA_9 address outputs and provide a new column address. This is only useful if the $\overline{ALE}$ input is Low, enabling the user to change addresses. This mode can be used with DRAMs that support page or nibble mode addressing.

Output driving characteristics:

Considering the transmission line characteristic of the DRAM arrays, the outputs of the IDC have been designed to provide incident-edge switching (in Dual-Inline-Packaged memory arrays), needed in high performance systems. For more information on the driving characteristics, please refer to Signetics application note number AN218. The driving characteristics of the 74F1763 are the same as those of the 74F765 shown in the application note.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	120	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current[1]			-15	mA
I_{OL}	Low-level output current[1]			24	mA
T_A	Operating free-air temperature range	0		70	°C

NOTE:
1. Transient currents will exceed these values in actual operation.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH2}[3] = -35mA	±5%V_{CC}	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
			I_{OL2}[4] = 60mA	±5%V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage	V_{CC}= MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Output current[5]	V_{CC} = MAX, V_O= 2.25V			-100		-225	mA
I_{CC}	Supply current (total)	V_{CC}= MAX					220	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{cc} = 5V, T_A = 25°C.
3. I_{OH2} is transient current necessary to guarantee a Low to High transition in a 70Ω transmission line.
4. I_{OL2} is transient current necessary to guarantee a High to Low transition in a 70Ω transmission line.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A=25°C, V_{cc}=+5.0V ±10%, C_L=300pF, RL=70Ω			T_A=0°C to +70°C, V_{cc}=+5.0V ±10%, C_L=300pF, RL=70Ω		
			Min	Typ	Max	Min	Max	
1	CP clock period (tcp)		10			10		ns
2	CP clock low time		5			5		ns
3	CP clock high time		5			5		ns
4	RCP clock period		100			100		ns
5	RCP clock low time		10			10		ns
6	RCP clock high time		10			10		ns
7	Setup time $\overline{REQ}$(↓) to CP(↑)		4	2		4		ns
8	$\overline{REQ}$ High hold time after CP(↑) **(Note 1)**		0			0		ns
9	$\overline{REQ}$ High pulse width **(Note 2)**		1/2tcp+5	1/2tcp+5	1/2tcp+5	1/2tcp+5	1/2tcp+5	ns
10	Propagation delay CP(↑) to GNT High		8.5	11	13.5	8.5	15.5	ns
11	Propagation delay $\overline{REQ}$(↑) to GNT Low		8.5	10.5	13	8.5	14	ns
12	$\overline{ALE}$ pulse width Low		4	1		4		ns
13	RA0-9,CA0-9 High or Low setup to $\overline{ALE}$(↑)		2	0		2		ns
14	$\overline{ALE}$(↑) to RA0-9,CA0-9 High or Low hold		1	0		1		ns
15	Propagation delay RA0-9,CA0-9 High or Low to MA0-9 **(Note 3)**	$\overline{ALE}$ Low	4	7.5	11	4	14	ns
16	Propagation delay $\overline{ALE}$(↓) to MA0-9		5.5	8.5	13	5.5	15	ns
17	Propagation delay CP(↑) to $\overline{RAS}$(↓)		8.5	10.5	12.5	8.5	14	ns
18	$\overline{RAS}$(↓) to MA0-9 (colum address) skew	HLDROW = 1	1/2tcp-2	1/2tcp+2	1/2tcp+5.5	1/2tcp-2.5	1/2tcp+7	ns
19	$\overline{RAS}$(↓) to MA0-9 (column address) skew	HLDROW = 0	1tcp-2	1tcp+2	1tcp+5.5	1tcp-2.5	1tcp+7	ns
20	$\overline{RAS}$(↓) to $\overline{RAS}$(↑) skew	PAGE = 1	4tcp+1.5	4tcp+3.5	4tcp+6	4tcp+1	4tcp+6.5	ns
21	Propagation delay CP(↑) to $\overline{RAS}$(↑)		12	14	16.5	12	18.5	ns
22	Propagation delay $\overline{REQ}$(↑) to $\overline{RAS}$(↑) **(Note 4)**		14.5	17.5	20	14	24	ns
23	Propagation delay CP(↓) to $\overline{CAS}$(↓)		6	8	10	6	11	ns
24	Propagation delay $\overline{PAGE}$(↑) to $\overline{RAS}$(↑) **(Note 4)**		10	12.5	15	10	17	ns
25	$\overline{RAS}$(↓) to $\overline{CAS}$(↓) skew		1.5tcp-4.5	1.5tcp-2.5	1.5tcp-o.5	1.5tcp-5.5	1.5tcp	ns
26	Propagation delay $\overline{REQ}$(↑) to $\overline{CAS}$(↑)		10	12	15	10	17	ns
27	MA0-9 (column address) to $\overline{CAS}$(↓) skew		1tcp-8	1tcp-4	1tcp-0.5	1tcp-9	1tcp-0.5	ns

AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A=25°C V_{cc}=+5.0V±10% C_L=300pF RL=70Ω			T_A=0°C to +70°C V_{cc}=+5.0V±10% C_L=300pF RL=70Ω		
			Min	Typ	Max	Min	Max	
28	MA0-9 (column address) to $\overline{CAS}$(↓) skew	HLDROW = 0	1/2tcp-8	1/2tcp-4	1/2tcp-0.5	1/2tcp-9	1/2tcp-0.5	ns
29	Set-up time $\overline{PAGE}$(↓) to CP(↑)		2			2		ns
30	Propagation delay $\overline{REQ}$(↓) to $\overline{DTACK}$(↑)		6	8	11.5	6	12	ns
31	Propagation delay CP(↑) to $\overline{DTACK}$(↓)		7.5	9.5	12	7.5	13	ns
32	Propagation delay $\overline{REQ}$(↑) to $\overline{DTACK}$(3-state)		9	12	13	9	15.5	ns
33	MA0-9 (refresh address) to $\overline{RAS}$(↓) skew		1/2tcp-5			1/2tcp-6.5		ns
34	$\overline{RAS}$(↓) to MA0-9 (refresh addres) skew		1tcp-2			1tcp-2.5		ns
35	$\overline{RAS}$(↑) to RAS(↓) skew (precharge)	PRECHRG = 0	4tcp-6	4tcp-3.5	4tcp-1.5	4tcp-6.5	4tcp-6.5	ns
36	$\overline{RAS}$(↑) to RAS(↓) skew (precharge)	PRECHRG = 1	3tcp-6	3tcp-3.5	3tcp-1.5	3tcp+1	3tcp-6.5	ns

Note1: $\overline{REQ}$ High hold means that, if $\overline{REQ}$ is High at the rising clock edge, it is guaranteed that the $\overline{REQ}$ input was not samples as Low.
Note2: A 50% duty cycle clock is recommended. If the duty cycle of the clock is not 50%, $\overline{REQ}$ should be held high for enough time such that a falling CP clock edge samples $\overline{REQ}$ as High. This is to ensure that refresh cycles don't get locked-up.
Note3: When $\overline{ALE}$ is Low, the address input latches are in the transparant mode and therefore any changes in the address inputs will be propagated to the MA0-9 outputs. Figure 2 illustrates RA0-9 inputs propagating to the MA0-9 outputs, but later in the cycle, if $\overline{ALE}$ is still Low when the CA0-9 inputs are multiplexed to the MA0-9 outputs the CA0-9 inputs will be in the transparant mode.
Note4: If $\overline{PAGE}$ is High and $\overline{REQ}$ is Low, $\overline{RAS}$ is automatically negated after approximately 4 CP clock cycles. If $\overline{PAGE}$ is Low and $\overline{REQ}$ is also Low, $\overline{RAS}$ will be negated when $\overline{PAGE}$ goes High. $\overline{RAS}$ will always be negated when $\overline{REQ}$ goes High regardless of the state of $\overline{PAGE}$ input.

TIMING DIAGRAMS

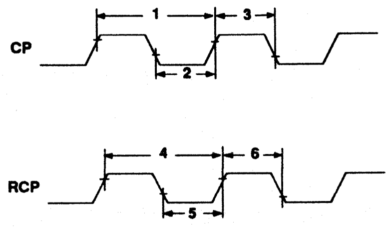


Figure 1: Clock cycle Timing

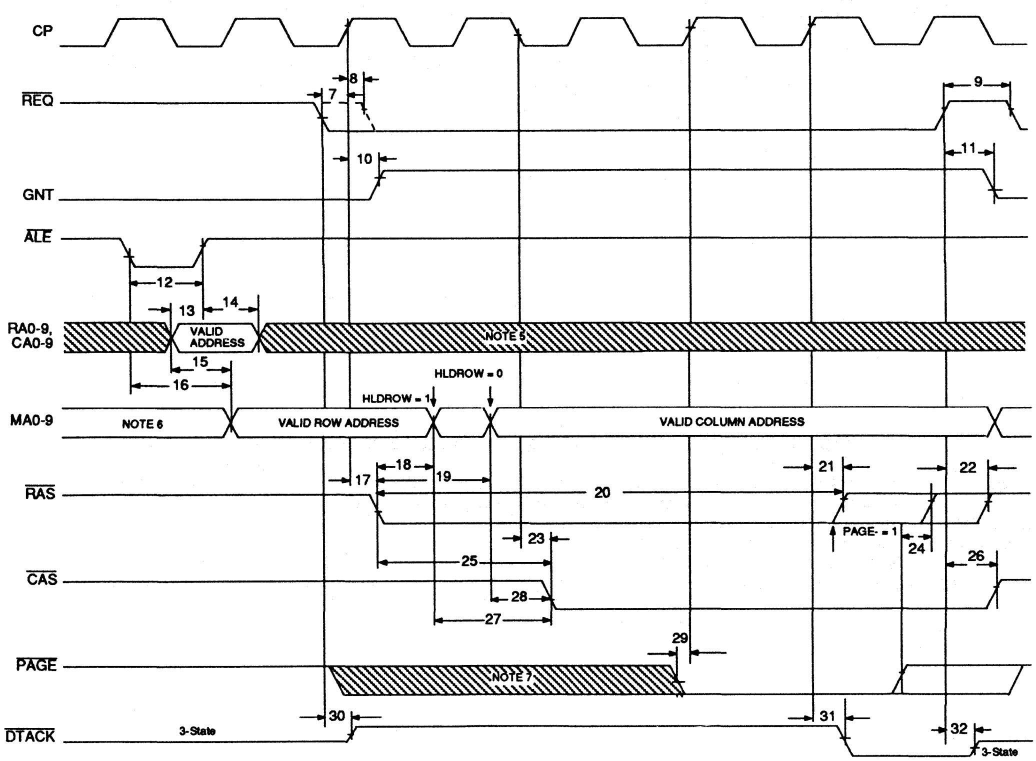


Figure 2: Memory access cycle timing

Note 5: If the RA0-9 & CA0-9 address inputs are not latched,RA0-9 inputs should remain valid until row address hold time is met and CA0-9 inputs should remain valid until column address hold time is met.
Note 6: MA0-9 outputs will contain the present row address on the RA0-RA9 inputs or the last row address latched into the device.
Note 7: PAGE input may be asserted anytime before this rising clock edge inorder to hold RAS Low.

TIMING DIAGRAM

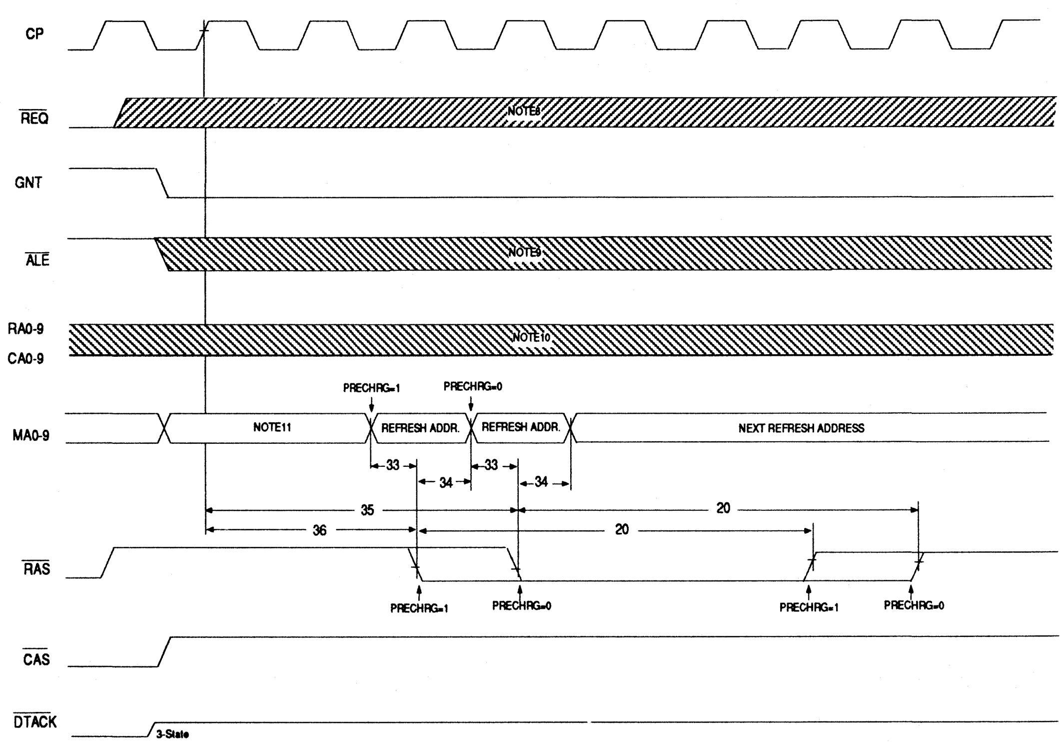


Figure 3: Refresh cycle timing following a memory access cycle

Note 8: $\overline{REQ}$ input is a don't care during a memory refresh cycle. If $\overline{REQ}$ is asserted during a refresh cycle, it will be recognized at the first rising CP clock edge, following the refresh cycle and it's associated $\overline{RAS}$ precharge time (see Figure 4).
Note 9: RA0-9 & CA0-9 address inputs may be latched at anytime during a memory refresh cycle. However, a memory access cycle will not begin until after the completion of the refresh cycle.
Note 10: RA0-9 & CA0-9 if in the transparant mode do not propagate to the MA0-9 outputs during a refresh cycle.
Note 11: MA0-9 outputs will contain the present row address on the RA0-RA9 inputs or the last row address latched into the device.

TIMING DIAGRAM

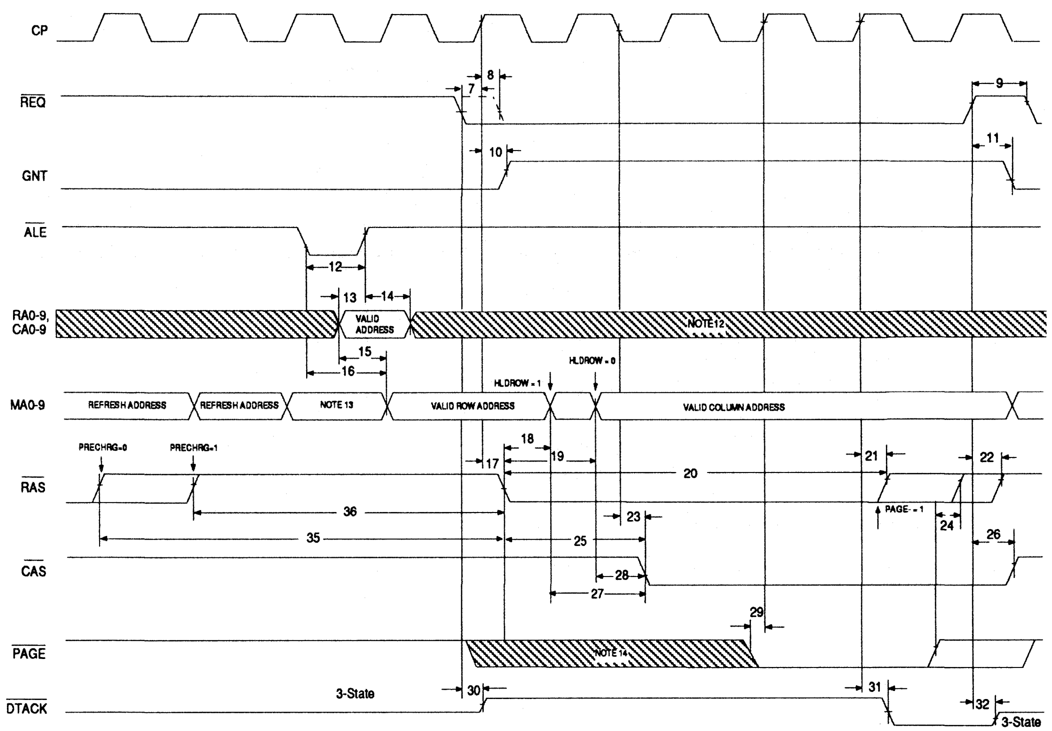


Figure 4: Memory access cycle timing following a refresh cycle

Note 12: If the RA0-9 & CA0-9 address inputs are not latched,RA0-9 inputs should remain valid until row address hold time is met and CA0-9 inputs should remain valid until column address hold time is met.
Note 13: MA0-9 outputs will contain the present row address on the RA0-RA9 inputs or the last row address latched into the device.
Note 14: $\overline{PAGE}$ input may be asserted anytime before this rising clock edge inorder to hold $\overline{RAS}$ Low.

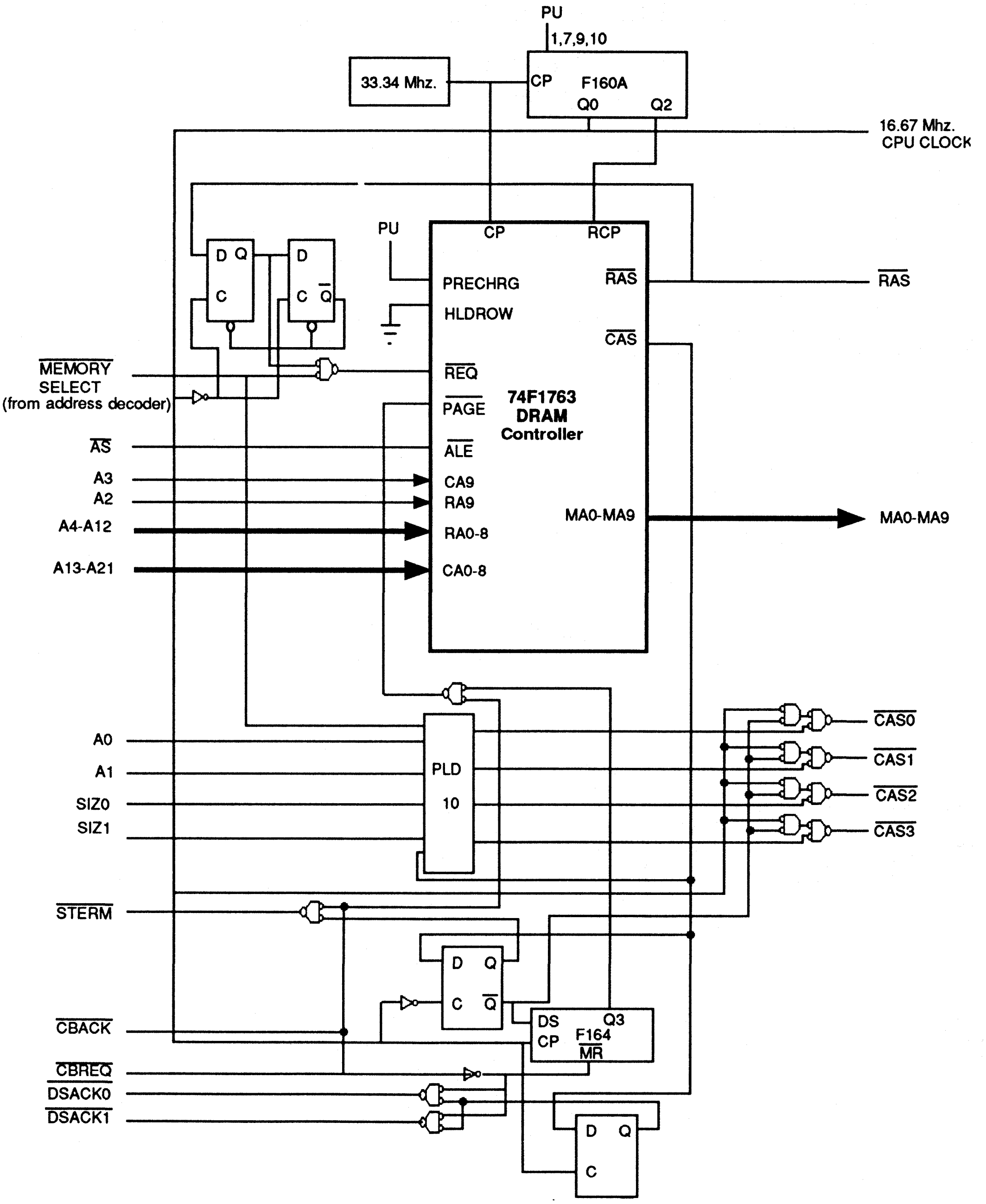


Figure 5: 16.67 MHz 68030 interface with 74F1763 for cache burst mode support using 4Mbytes of 100nsec. nibble-mode DRAMs (Four 32bit words read to or written from cache in only 7 clock cycles).

FAST 74F1764/1765
74F1764-1/1765-1
I Megabit DRAM Dual-Ported Controller

FAST Products

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1764/1765	150MHz	150mA
74F1764-1/1765-1	150MHz	125mA

FEATURES

- Allows two microprocessors to access the same bank of dynamic RAM
- Performs arbitration, signal timing, address multiplexing and refresh
- 10 address output pins allow direct control of up to 1Mbit dynamic RAMs
- External address multiplexing enables control of 4Mbit (or greater) dynamic RAMs
- Separate refresh clock allows adjustable refresh timing
- 74F1764/F1764-1 have on-chip 20-bit address input latch
- Allows control of dynamic RAMS with row access times down to 40ns
- 74F1764/F1765 output drivers designed for incident wave switching
- 74F1764-1/F1765-1 output drivers designed for first reflected wave switching

DESCRIPTION

The 74F1764/1765 DRAM Dual-ported Controller is a high speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing device to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

74F1764 vs 74F1765

The 74F1764 though functionally and pin to pin compatible with the 74F1765 differs from the later in that it has an on-chip address input latch. This is useful in systems that have unlatched or multiplexed address and data bus.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V\pm10\%$; $T_A = 0°C$ to $+70°C$
48-Pin Plastic DIP	N74F1764N, N74F1765N, N74F1764-1N, N74F1765-1N
44-Pin PLCC	N74F1764A, N74F1765A, N74F1764-1A, N74F1765-1A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
RA_0 - RA_9		Row address inputs	1.0/1.0	20µA/0.6mA
CA_0 - CA_9		Column address inputs	1.0/1.0	20µA/0.6mA
$\overline{REQ}_1$, $\overline{REQ}_2$		Memory access request inputs	1.0/1.0	20µA/0.6mA
CP		Clock input	1.0/1.0	20µA/0.6mA
RCP		Refresh clock input	1.0/1.0	20µA/0.6mA
$\overline{SEL}_1$, $\overline{SEL}_2$	'F1764/1765	Select outputs	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
MA_0 - MA_9	'F1764/1765	Memory address outputs	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
GNT	'F1764/1765	Grant output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
$\overline{RAS}$	'F1764/1765	Row address strobe output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
WG	'F1764/1765	Write gate output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
$\overline{CASEN}$	'F1764/1765	Column address strobe enable output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
DTACK	'F1764/1765	Data transfer acknowledge output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	74F1764 74F1765	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7			V
V_{OH2}[3]				I_{OH2}[3]=-35mA	±5%V_{CC}	2.4			V
V_{OH}		74F1764-1 74F1765-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-20mA	±10%V_{CC}	2.4	2.7		V
					±5%V_{CC}	2.6	3.0		V
V_{OL}	Low-level output voltage	74F1764 74F1765	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{OL2}[3]				I_{OL2}[4]=60mA	±5%V_{CC}		0.45	0.80	V
V_{OL}		74F1764-1 74F1765-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=8mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{OL2}[3]				I_{OL2}[3]=75mA	±5%V_{CC}		2.1	2.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[5]	74F1764 74F1765	V_{CC} =MAX			-100		-225	mA
		74F1764-1 74F1765-1	V_{CC} =MAX			-60	100	-150	mA
I_{CC}	Supply current (total) I_{CCH}	74F1764 74F1765	V_{CC} =MAX				150	200	mA
	I_{CCL}						165	210	mA
	I_{CCH}	74F1764-1 74F1765-1					120	165	mA
	I_{CCL}						125	170	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Refer to Appendix A.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Document No.	853-
ECN No.	
Date of issue	June 4, 1990
Status	Product Specification
FAST Products	

FAST 74F1766
Burst Mode DRAM Controller (BMDC)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1766	150MHz	200mA

FEATURES

- Allows burst-mode access for systems using Nibble/Page/Static column mode DRAMs
- Complete control of DRAM access, acknowledge, refresh and address multiplexing functions
- True $\overline{RAS}$ interleaving for minimum refresh and $\overline{RAS}$ precharge overhead
- Asynchronous arbitration to speed up accesses
- Selectable Precharge and Acknowledge times
- Selectable Row address hold times
- Supports $\overline{CAS}$ before $\overline{RAS}$ refresh
- Allows control of dynamic RAMs with row access times down to 30ns
- Output drivers designed for incident wave switching

DESCRIPTION

The Philips Burst Mode DRAM Controller (BMDC) is a high performance memory timing generator designed to support Page, Nibble or Static Column modes of operation in addition to the normal DRAM access cycles. It performs memory access/refresh arbitration, refresh and memory access timing, $\overline{RAS}$ interleaving, $\overline{CAS}$ byte decoding and controls up to four banks of DRAM.

The BMDC generates DRAM timing and thus requires a companion address multiplexer like the 74F1762 Memory Address Multiplexer for row and column address generation. This provides the flexibility of using the controller with any size of DRAM array by simply using an appropriate address multiplexer. For example when used with the 74F1762, it can control 4Mbit DRAMs.

ORDERING INFORMATION

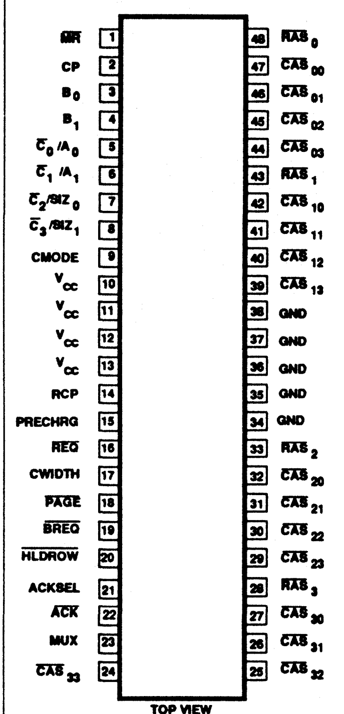
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V\pm10\%$; $T_A = 0°C$ to $+70°C$
48-Pin Plastic DIP	N74F1766N
44-Pin PLCC	N74F1766A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

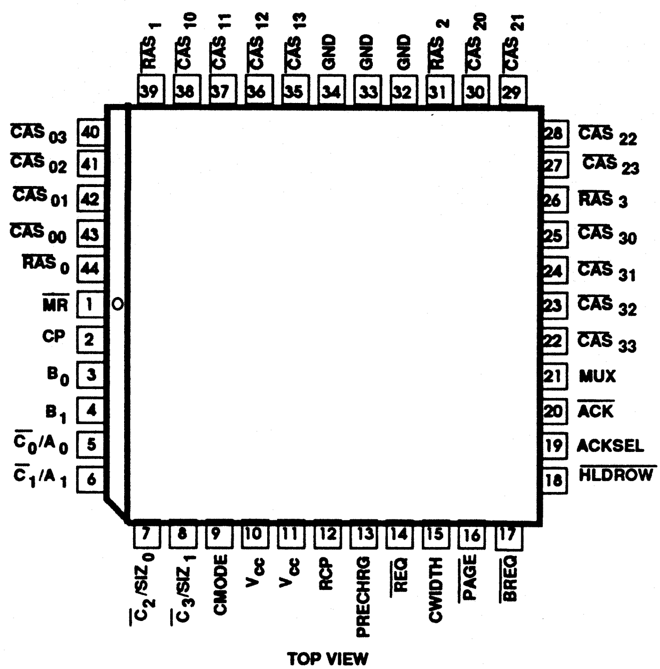
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{C}_0/A_0$, $\overline{C}_1/A_1$, $\overline{C}_2/SIZ_0$, $\overline{C}_3/SIZ_1$,	$\overline{CAS}$ Enable inputs	1.0/1.0	20µA/0.6mA
PRECHRG	$\overline{RAS}$ Precharge Select Input	1.0/1.0	20µA/0.6mA
$\overline{REQ}$	Memory access request input	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
RCP	Refresh clock input	1.0/1.0	20µA/0.6mA
B_0, B_1	Bank select inputs	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Reset input	1.0/1.0	20µA/0.6mA
$\overline{BREQ}$	Burst request input	1.0/1.0	20µA/0.6mA
ACKSEL	Acknowledge select input	1.0/1.0	20µA/0.6mA
$\overline{HLDROW}$	Row address hold select input	1.0/1.0	20µA/0.6mA
$\overline{PAGE}$	Page mode select input	1.0/1.0	20µA/0.6mA
CMODE	$\overline{CAS}$ mode select input	1.0/1.0	20µA/0.6mA
CWIDTH	$\overline{CAS}$ width select input	1.0/1.0	20µA/0.6mA
$\overline{ACK}$	Acknowledge output	750/40	3.0mA/24mA
MUX	Address Multiplexer output	150/40	15.0mA/24mA
$\overline{RAS}_{0-3}$	Row address strobe outputs	750/40	15.0mA/24mA
$\overline{CAS}_{00-33}$	Column address strobe outputs	750/40	15.0mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state

DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
CP	2	2	Input	Clock input. Used by the controller for all timing and arbitration functions.
RCP	14	12	Input	Refresh clock input. Divided internally by 64 to produce an internal Refresh Requst.
PRECHRG	15	13	Input	$\overline{RAS}$ Precharge input. A Low will program the Controller to guarantee 4 CP clock cycles of precharge. A High will guarantee 3 clock cycles of precharge.
$\overline{REQ}$	16	14	Input	Active Low Memory Access Request input, must be asserted for the entire DRAM access cycle. $\overline{REQ}$ is sampled on the rising edge of the CP clock.
B_0,B_1	3,4	3,4	Input	$\overline{RAS}$ Bank Select inputs.See Table1 for decoding information.
$\overline{BREQ}$	19	17	Input	Active Low Burst Request input. If active during an access cycle, the controller automatically toggles $\overline{CAS}_X$ outputs for burst access. The duration of the $\overline{CAS}_X$ outputs are controlled by the CWIDTH and $\overline{PAGE}$ inputs.
ACKSEL	21	19	Input	Acknowledge timing Select input. A Low will program the Controller to assert $\overline{ACK}$ output 2 CP clock cycles after $\overline{CAS}_X$ is asserted. When High $\overline{ACK}$ output will be asserted at the time of assertion of $\overline{CAS}_X$.
$\overline{HLDROW}$	20	18	Input	Row Address Hold input. A Low will program the Controller to assert MUX output 1/2 CP clock cycles after $\overline{RAS}_X$ is asserted. When High MUX output will be asserted at the time of assertion of $\overline{RAS}_X$.
$\overline{ACK}$	22	20	Output	Active Low, 3-state Acknowledge output. Asserted as selected by the ACKSEL input. This is asserted only once during a burst or non-burst memory access cycle, and is not asserted during a memory refresh cycle.
CMODE	9	9	Input	$\overline{CAS}$ Mode select input. When Low $\overline{CAS}_X$ outputs are enabled directly by the $\overline{C}_{0-3}$ inputs. When High $\overline{CAS}_X$ outputs are enabled by decoding the A_{0-1} and SIZ_{0-1} inputs (see Table 2).
$\overline{C}_0/A_0$	5	5	Input	$\overline{CAS}_{X0}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{C}_1/A_1$	6	6	Input	$\overline{CAS}_{X1}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{C}_2/SIZ_0$	7	7	Input	$\overline{CAS}_{X2}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{C}_3/SIZ_1$	8	8	Input	$\overline{CAS}_{X3}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{RAS}_{0-3}$	48,43, 33,28	44,39, 31,26	Output	Active Low Row Address Strobe outputs. Asserted as dictated by the B_{0-1} inputs. (see Table 1 for decoding information)
CWIDTH	17	15	Input	$\overline{CAS}_X$ pulse Width select input. This input selects the initial $\overline{CAS}_X$ pulse width in the burst mode. When Low the initial $\overline{CAS}_X$ pulse is selected equal to 3 CP clock cycles and when High it's selected equal to 2 CP clock cycles. This input is ignored in the non-burst mode.
MUX	23	21	Output	Row/Column address Multiplex output. Asserted as selected by the $\overline{HLDROW}$ input and is used by an external address multiplexer like the 74F1762.
$\overline{CAS}_{00-33}$	47-44, 42-39, 32-29, 27-24	43-40, 38-35, 30-27, 25-22	Output	Active Low Column Address Strobe outputs. Asserted when enabled by the $\overline{CAS}_X$ enable inputs (Table 2) and $\overline{RAS}_X$ bank circuitry.
$\overline{PAGE}$	18	16	Input	$\overline{PAGE}$ mode select input. Controls $\overline{CAS}_X$ pulse width after the initial $\overline{CAS}_X$ pulse in the burst mode. When this input is Low the $\overline{CAS}_X$ pulse is selected equal to 2 CP cycles and when High it's selected equal to 1 CP cycle. This is ignored in the non-burst mode.
$\overline{MR}$	1	1	Input	Active Low Master Reset input. The first Low to High transition on the CP clock after $\overline{RESET}$ is Low will reset the controller. After reset, the 74F1766 remains in test mode until the first rising edge of CP clock.
Vcc	10-13	10,11		Power
GND	34-38	32-34		Ground

ARCHITECTURE

The 74F1766 Burst Mode DRAM controller is a synchronous device, with all signal generation being a function of the input clock (CP).

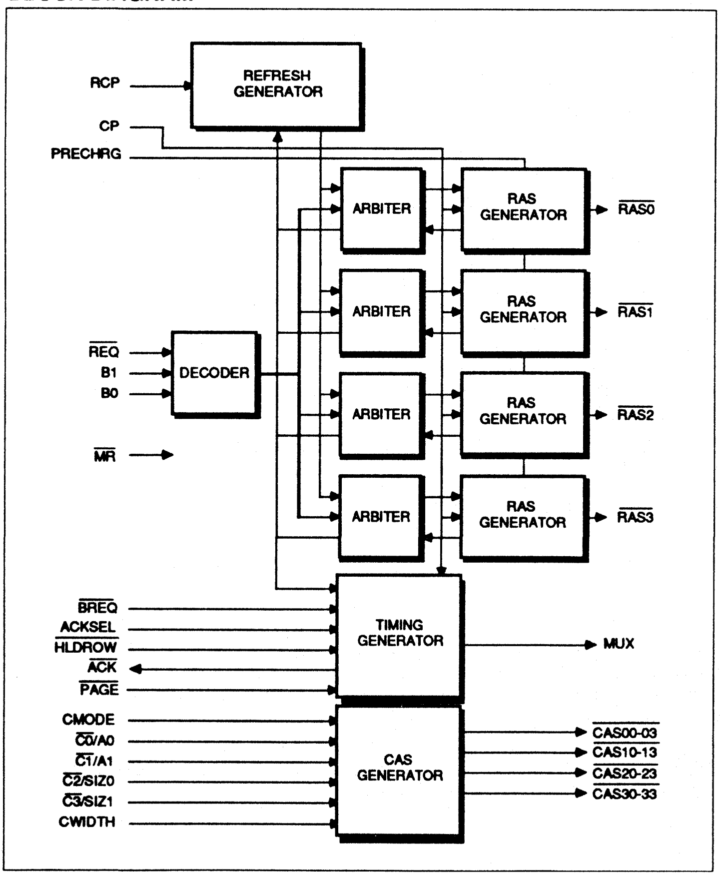
The 'F1766 Block Diagram (Figure 1) shows the overall architecture of the device. The refresh generator uses $\overline{CAS}$ before $\overline{RAS}$ refresh and produces refresh requests based upon the frequency of the refresh clock (RCP). A memory refresh request is generated for all four banks every 64 cycles of the RCP clock. This request is arbitrated individually for all banks with it's corresponding memory access request made through the $\overline{REQ}$ input. If both memory access and refresh requests are active at a given time the request sampled first will begin immediately and the other request (if still asserted) will be serviced upon completion of the current cycle and it's associated precharge time.

Every one of the four banks have individual refresh monitors to keep track of any missed refreshes during a long page mode access. A total of 127 missed refreshes can be stored by each bank. After the page mode access cycle the controller will burst refresh that bank until all missed refreshes have been performed. In order to limit the number of outputs switching at the same time the refresh generator will stagger the refresh cycles to individual banks, starting from Bank 0. The bank select inputs (B_{0-1}) select which $\overline{RAS}_x$ output will be enabled during the access cycle. Each $\overline{RAS}_x$ output has it's own arbiter and timing generator to allow true $\overline{RAS}$ interleaving between access cycles and refresh cycles. This also enables transparant $\overline{RAS}$ precharge between access cycles. The $\overline{RAS}$ precharge time can be selected by the PRECHRG input to be equal to either 3 or 4 CP clock cycles.

The timing generator allows burst or non-burst accesses selected by the $\overline{BREQ}$ input. If $\overline{BREQ}$ input is asserted during a memory access cycle the controller will automatically toggle $\overline{CAS}_x$ outputs for burst accesses. The duration of the first $\overline{CAS}_x$ pulse is determined by the CWIDTH input, and by the $\overline{PAGE}$ input for subsequent $\overline{CAS}_x$ pulses. This is particularly useful when block moves are made into and out of memory for cache transfers. The $\overline{CAS}_x$ outputs may be gated by the byte select inputs ($\overline{C}_{0-3}$) or by a decoding function generated by the $A_0/A_1/SIZ_0/SIZ_1$ using the CMODE input. Each $\overline{RAS}$ output has an associated set of $\overline{CAS}$ outputs for that bank, for example $\overline{RAS}_0$ uses $\overline{CAS}_{00-03}$ outputs. This allows simultaneous refresh of $\overline{RAS}$ banks while another bank is being accessed by the processor.

The ACKSEL input allows the assertion of Acknowledge ($\overline{ACK}$) output to be either when $\overline{CAS}_x$ is asserted or 2 CP clock cycles after that. $\overline{ACK}$ stays asserted in the burst mode until $\overline{REQ}$ is negated. The $\overline{HLDROW}$ input can be used to assert MUX output when $\overline{RAS}_x$ is asserted or one-half CP clock cycle after that.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Most DRAMs require that $\overline{RAS}$ and $\overline{CAS}$ inputs be toggled a number of times before the DRAM may be used. The BMDC has an initialization feature which allows the automatic excersizing of the DRAMs. This is done by resetting the device, which forces the refresh counter to be offset by ten, thus forcing ten refresh cycles before allowing any memory access cycles. The $\overline{REQ}$ input is sampled on the rising edge of the CP clock. If no refresh request is being serviced, one of the $\overline{RAS}_x$ outputs (depending on the B_{0-1} inputs) will be asserted immediately. Depending on the state of the $\overline{HLDROW}$ input, the MUX output will be driven High either at the assertion of $\overline{RAS}_x$ or one-half CP cycle after that. One CP cycle after the assertion of $\overline{RAS}_x$, the $\overline{CAS}_x$ outputs enabled either by the $\overline{C}_{0-3}$ inputs or the decoded function of $A_0/A_1/SIZ_0/SIZ_1$ (as selected by the CMODE input) will be asserted. If the ACKSEL input is High, the $\overline{ACK}$ output will be asserted at this time; otherwise it will be asserted 2 CP cycles after this time.

The $\overline{BREQ}$ input is sampled when the $\overline{CAS}_x$ outputs are initially asserted, and this determines what will take place on the $\overline{CAS}_x$ outputs after their initial assertion. If $\overline{BREQ}$ is High, the $\overline{RAS}_x$, MUX and $\overline{CAS}_x$ outputs will remain in their present state until the negation of $\overline{REQ}$, at which time all these signals are negated. Negation of $\overline{REQ}$ is asynchronous to the CP clock cycle and therefore is not sampled by the clock. If the $\overline{BREQ}$ is Low at the assertion of $\overline{CAS}_X$, the $\overline{RAS}_X$ and MUX outputs will stay in their existing state but the $\overline{CAS}_X$ outputs after staying Low for 2 CP cycles will alternately be negated and asserted for one CP clock cycle if $\overline{PAGE}$ input is High or for two CP clock cycles if $\overline{PAGE}$ input is Low. This process will continue untill the negation of the $\overline{REQ}$ input, at which time the $\overline{RAS}_X$, MUX, $\overline{CAS}_X$ and $\overline{ACK}$ outputs will be negated.

As mentioned before, the controller guarantees a $\overline{RAS}$ precharge on all the $\overline{RAS}_X$ outputs to be either 3 or 4 CP clock cycles as selected by the PRECHRG input. This precharge function is independent among the $\overline{RAS}_X$ outputs, which means that, by connecting the appropriate low-order address lines from the processor to the $B_{0\text{-}1}$ inputs, sequential accesses, a common occurance with microprocessors, will result in no precharge overhead.

The refresh function is also independent between the $\overline{RAS}_X$ outputs, which means that three $\overline{RAS}_X$ outputs can be performing a $\overline{CAS}$ before $\overline{RAS}$ refresh, while the fourth is in the precharge mode or is being accessed, thus reducing the overall refresh overhead.

Output driving Characteristics

Considering the transmission line characteristics of the DRAM arrays, the outputs of the DRAM controller have been designed to provide incident-edge switching (in Dual-Inline-Packaged memory arrays), needed in high performance systems. For more information on the driving characteristics, please refer to Signetics application note number AN218. The driving characteristics of the 74F1766 are the same as those of the 74F765 shown in the application note.

Testing the BMDC

Precautions have been taken in the design of the BMDC to facilitate testing of the device. After a $\overline{MR}$ is issued and the CP input is toggled from Low to High all internal flip-flops are brought into a known state, and the device goes into the test mode from the time $\overline{MR}$ is deasserted till the time the first Low to High transition occurs on the CP clock. During the test mode, bank refresh counters (that keep track of missed refreshes) are clocked by a High to Low transition on the $\overline{C}_{0\text{-}3}$ inputs and the main refresh counter is clocked on the rising RCP clock edge. The comparators that compare the contents of the main refresh counter and refresh counters of individual banks are clocked by the Low to High transition on the PRECHRG input and are gated on to $\overline{RAS}_X$ outputs by the $\overline{C}_{0\text{-}3}$ inputs. So whenever $\overline{C}_{0\text{-}3}$ are Low, $\overline{RAS}$ outputs are disabled (pulled High). If the contents of the main refresh counter and the individual bank counters are equal, the corresponding $\overline{RAS}$ output will be High, if not equal the corresponding $\overline{RAS}$ output will be Low. This allows full testing of the Counters and comparators with relatively few lines of code.

B_0	B_1	$\overline{RAS}_0$	$\overline{RAS}_1$	$\overline{RAS}_2$	$\overline{RAS}_3$
0	0	0	1	1	1
0	1	1	0	1	1
1	0	0	1	0	1
1	1	0	1	1	0

TABLE 1: BANK SELECT DECODE

CMODE	OPERATION	$\overline{C}_3/SIZ_1$	$\overline{C}_2/SIZ_0$	$\overline{C}_1/A_1$	$\overline{C}_0/A_0$	$\overline{CAS}_{X3}$	$\overline{CAS}_{X2}$	$\overline{CAS}_{X1}$	$\overline{CAS}_{X0}$
1		0	0	0	0	0	0	0	0
1	LONG WORD	0	0	0	1	0	0	0	1
1		0	0	1	0	0	0	1	1
1		0	0	1	1	0	1	1	1
1		0	1	0	0	1	1	1	0
1	BYTE	0	1	0	1	1	1	0	1
1		0	1	1	0	1	0	1	1
1		0	1	1	1	0	1	1	1
1		1	0	0	0	1	1	0	0
1	WORD	1	0	0	1	1	0	0	1
1		1	0	1	0	0	0	1	1
1		1	0	1	1	0	1	1	1
1		1	1	0	0	1	0	0	0
1	THREE BYTES	1	1	0	1	0	0	0	1
1		1	1	1	0	0	0	1	1
1		1	1	1	1	0	1	1	1

TABLE 2: BYTE SELECT DECODE

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	All pins except $\overline{ACK}$			-15	mA
		$\overline{ACK}$ output			-3	mA
I_{OL}	Low-level output current				24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	All pins except $\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.5	3.2		V
					±5%V_{CC}	2.7	3.4		V
V_{OH2}[3]				I_{OH2}[3]=-35mA	±5%V_{CC}	2.4			V
V_{OH}		$\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=MAX	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	All pins except $\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{OL2}[3]				I_{OL2}[3]=60mA	±5%V_{CC}		0.45	0.80	V
V_{OL}		$\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V					-0.6	mA
I_{OZH}	Off-state output current, High level voltage applied		V_{CC} =MAX, V_o = 2.7V					50	µA
I_{OZL}	Off-state output current, Low level voltage applied		V_{CC} =MAX, V_o = 0.5V					-50	µA
I_{OS}[4]	Short-circuit output current		V_{CC} =MAX	All pins except $\overline{ACK}$		-100		-225	mA
				$\overline{ACK}$ output		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} =MAX				185	240	mA
		I_{CCL}					200	260	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH}[2] & I_{OL}[2] are transient currents necessary to guarantee a Low to High & a High to Low transition in a 30 OHM transmission line respectively. Refer to Application note number AN218 for further explanation.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

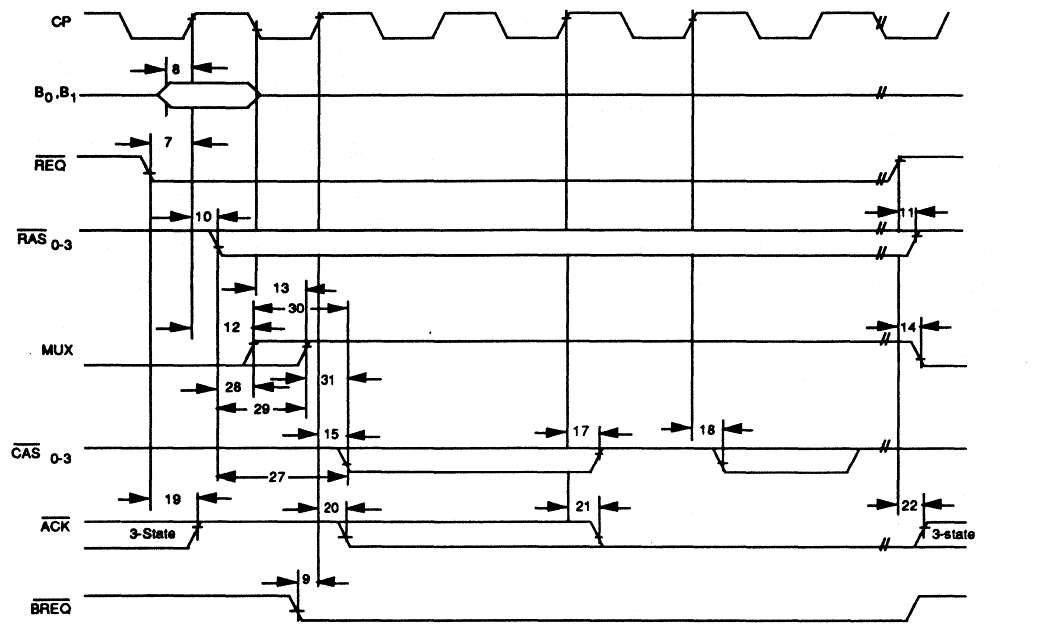
AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A=25°C, V_{cc}=+5.0V ±10%, C_L=300pF, RL=70Ω			T_A=0°C to +70°C, V_{cc}=+5.0V ±10%, C_L=300pF, RL=70Ω		
			Min	Typ	Max	Min	Max	
1	CP clock period (tcp)		10			10		ns
2	CP clock low time		4			4		ns
3	CP clock high time		6			6		ns
4	RCP clock period		100			100		ns
5	RCP clock low time		10			10		ns
6	RCP clock high time		10			10		ns
7	Setup time $\overline{REQ}$(↓) to CP(↑)		2.5			4		ns
8	Setup time B_0, B_1 to CP(↑)		3			4		ns
9	Setup time $\overline{BREQ}$ to CP(↑)		3			4		ns
10	Propagation delay CP(↑) to $\overline{RAS}$(↓)		3	7.5	9.5	3	10	ns
11	Propagation delay $\overline{REQ}$(↑) to $\overline{RAS}$(↑)		4	9	12	3	13	ns
12	Propagation delay CP(↑) to MUX(↑)	$\overline{HLDROW}$ = 1	3	8	10	3	11	ns
13	Propagation delay CP(↓) to MUX(↑)	$\overline{HLDROW}$ = 0	2	5.5	7.5	2	8.5	ns
14	Propagation delay $\overline{REQ}$(↑) to MUX(↓)		4	8.5	10.5	4	11.5	ns
15	Propagation delay CP(↑) to $\overline{CAS}$(↓)		3	8.5	11.5	3	12	ns
16	Propagation delay $\overline{REQ}$(↑) to $\overline{CAS}$(↑)		4	9.5	12	4	14	ns
17	Propagation delay CP(↑) to $\overline{CAS}$(↑)	$\overline{BREQ}$ = 0	3	8	10	3	11	ns
18	Propagation delay CP(↑) to $\overline{CAS}$(↓)	$\overline{BREQ}$ = 0	3	9	11	3	12	ns
19	Propagation delay $\overline{REQ}$(↓) to $\overline{ACK}$(3-state to High)		2	5	7	2	8	ns
20	Propagation delay CP(↑) to $\overline{ACK}$(↓)	ACKSEL = 1	3	7.5	9.5	3	10	ns
21	Propagation delay CP(↑) to $\overline{ACK}$(↓)	ACKSEL = 0	3	7.5	9.5	3	10	ns
22	Propagation delay $\overline{REQ}$(↑) to $\overline{ACK}$(Low to 3- state)		2	5	7	2	7.5	ns
23	Propagation delay CP(↑) to $\overline{CAS}$(↓) *	REFRESH CYCLE	4	9.5	12	4	13	ns
24	Propagation delay CP(↑) to $\overline{RAS}$(↓) *	REFRESH CYCLE	3	7.5	9.5	3	10	ns
25	Propagation delay CP(↑) to $\overline{CAS}$(↑) *	REFRESH CYCLE	4	9.5	12	4	14	ns
26	Propagation delay CP(↑) to $\overline{RAS}$(↑) *	REFRESH CYCLE	4	9	11	3	13	ns
27	Propagation delay $\overline{RAS}$(↓) to $\overline{CAS}$(↓)		1tcp-1	1tcp+1	1tcp+2.5	1tcp-1	1tcp+3	ns

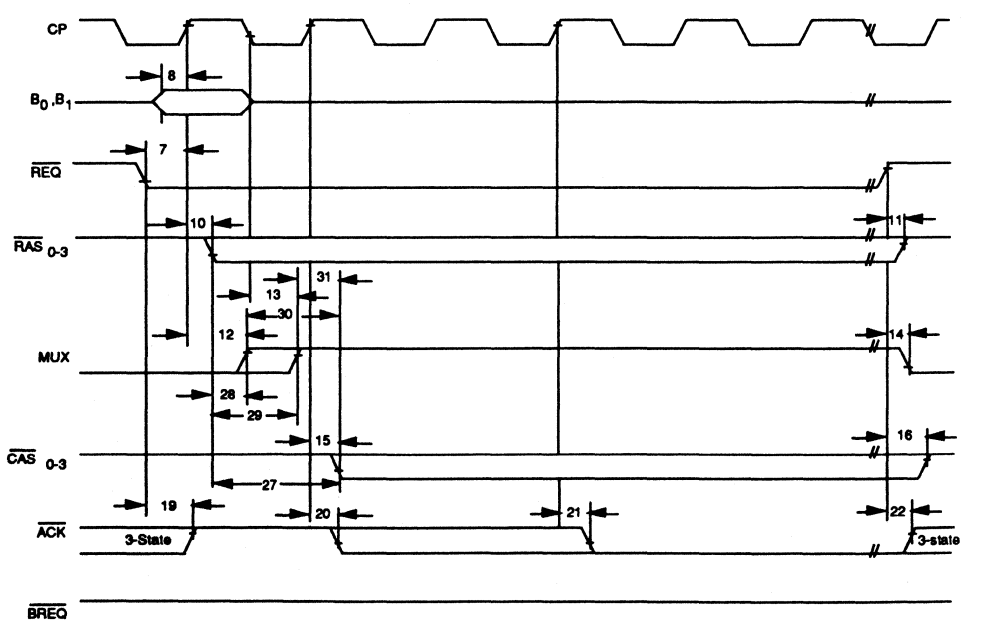
* The same parameters will hold for a refresh cycle during $\overline{RAS}_1$, $\overline{RAS}_2$ and $\overline{RAS}_3$ access cycles.

AC ELECTRICAL CHARACTERISTICS

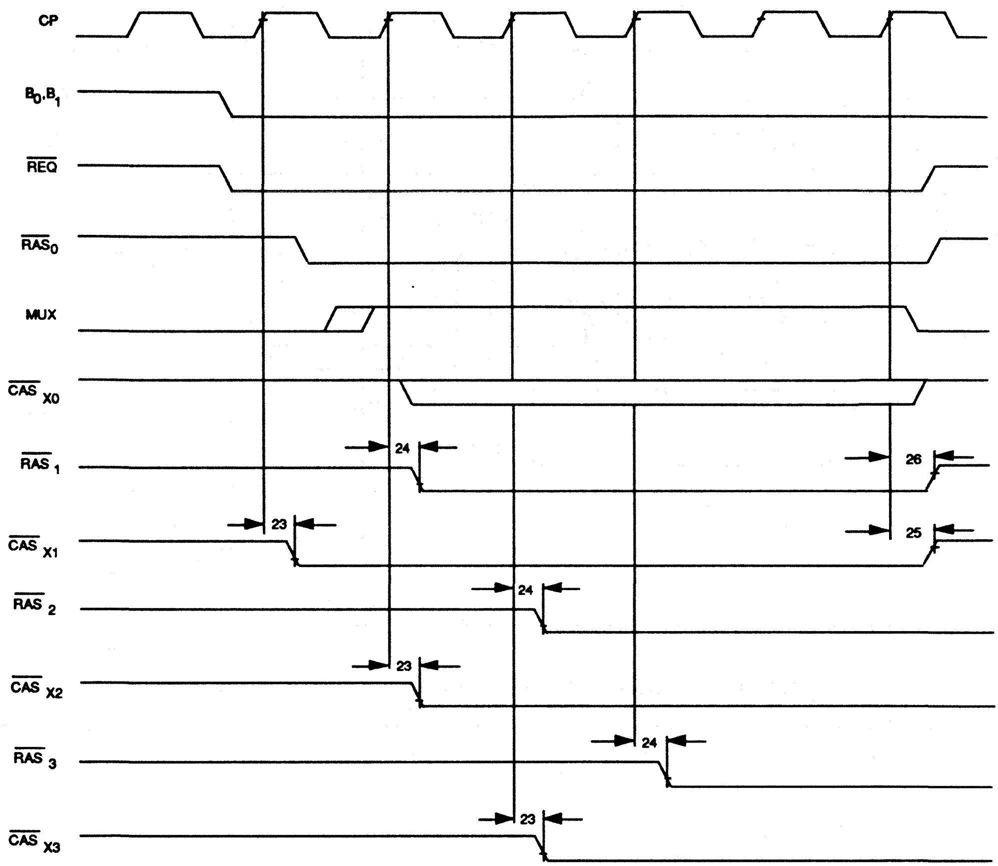
NO	PARAMETER	TEST CONDITIONS	LIMITS T_A=25°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω			LIMITS T_A=0°C to +70°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω		UNIT
			Min	Typ	Max	Min	Max	
28	Propagation delay $\overline{RAS}$(↓) to MUX(↑)	HLDROW = 1	-1	0.5	2	-1.5	2.5	ns
29	Propagation delay $\overline{RAS}$(↓) to MUX(↑)	HLDROW = 0	1/2tcp-3.5	1/2tcp-1.5	1/2tcp	1/2tcp-1.5	1/2tcp+2.5	ns
30	Propagation delay MUX(↑) to $\overline{CAS}$(↓)	HLDROW = 1	1tcp-1.5	1tcp+0.5	1tcp+2	1tcp-2.5	1tcp+2.5	ns
31	Propagation delay MUX(↑) to $\overline{CAS}$(↓)	HLDROW = 0	1/2tcp+0.5	1/2tcp+2	1/2tcp+4.5	1/2tcp-0.5	1/2tcp+5	ns



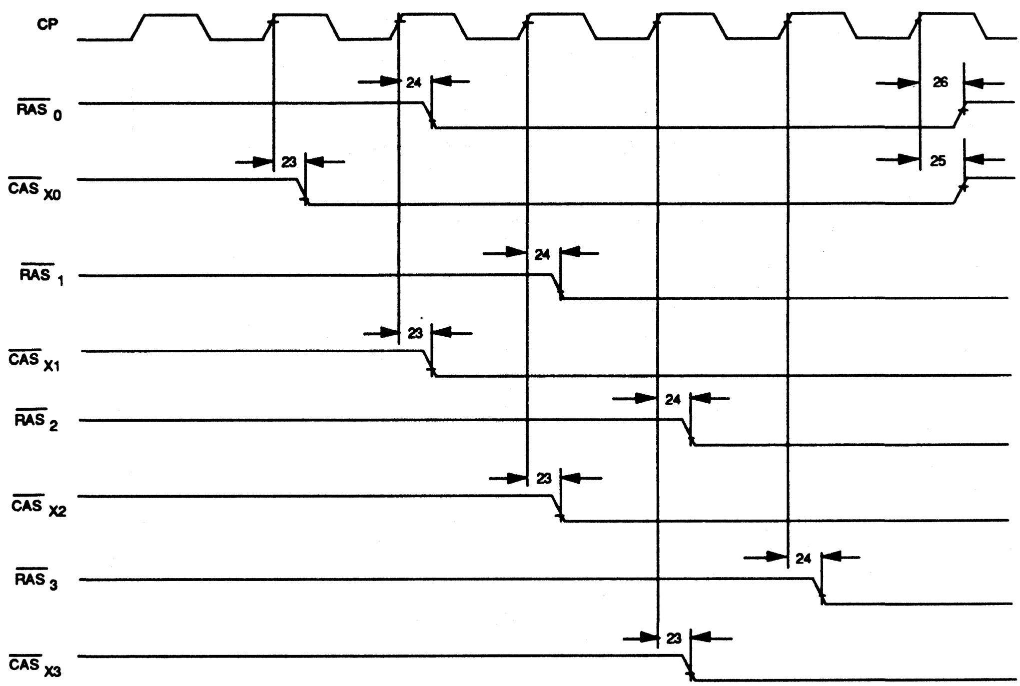
Waveform 1: Burst mode access timing



Waveform 2: Non-Burst mode access timing

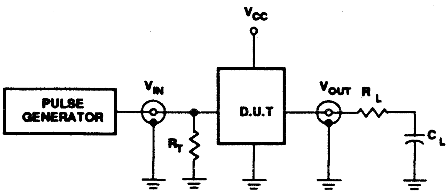


Waveform 3: Refresh cycle timing during $\overline{RAS}_0$ access

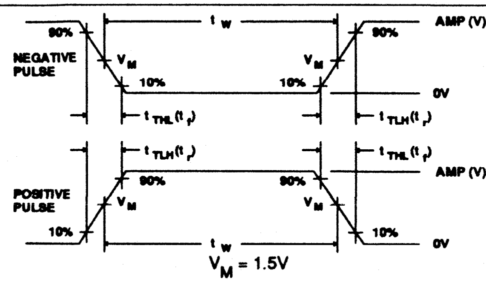


Waveform 4: Refresh cycle timing when memory is not being accessed

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-1097
ECN No.	97708
Date of issue	September 22, 1989
Status	Product Specification
FAST Products	

FAST 74F2952, 74F2953 Transceivers

74F2952 Registered Transceiver, Non-Inverting (3-State)
74F2953 Registered Transceiver, Inverting (3-State)

FEATURES

- **8-bit Registered Transceivers**
- **Two 8-bit, back-to-back registers store data moving in both directions between two bidirectional busses**
- **Separate Clock, Clock Enable and 3-state Enable provided for each register**
- **'F2952 Non-Inverting 'F2953 Inverting**
- **AM2952/2953 functional equivalent**
- **A outputs sink 24mA and source 3mA**
- **B outputs sink 64mA and source 15mA**
- **300 mil wide 24-pin Slim DIP package**

DESCRIPTION

The 74F2952 and 74F2953 are 8-bit Registered Transceivers. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-state output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F2952	160MHz	105mA
74F2953	160MHz	105mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F2952N, N74F2953N
24-Pin Plastic SOL[1]	N74F2952D, N74F2953D
28-Pin Plastic PLCC	N74F2952A, N74F2953A

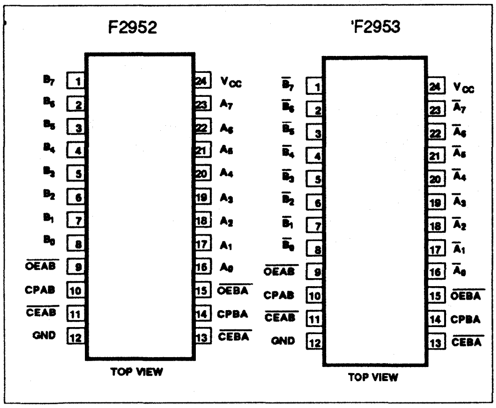
NOTE:
1. Thermal mounting techniques are recommended.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

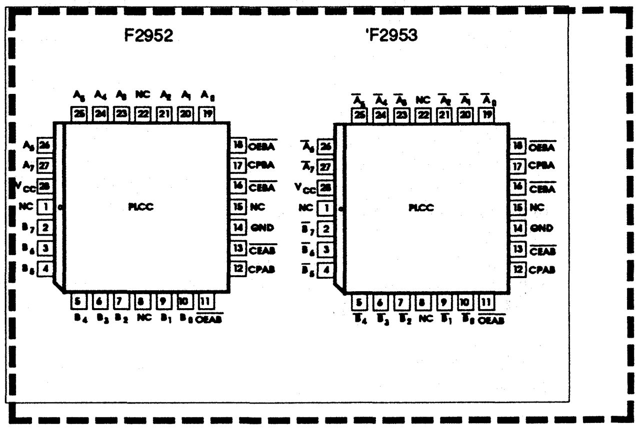
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	Port A, 3-state inputs	3.5/1.0	70µA/0.6mA
$B_0 - B_7$	Port B, 3-state inputs	3.5/1.0	70µA/0.6mA
CPAB,CPBA	Clock inputs	1.0/1.0	20µA/0.6mA
$\overline{CEAB}$,$\overline{CEBA}$	Clock Enable inputs	1.0/1.0	20µA/0.6mA
$\overline{OEAB}$,$\overline{OEBA}$	Output Enable inputs	1.0/1.0	20µA/0.6mA
$A_0 - A_7$	Port A, 3-state outputs	150/40	3.0mA/24mA
$B_0 - B_7$	Port B, 3-state outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

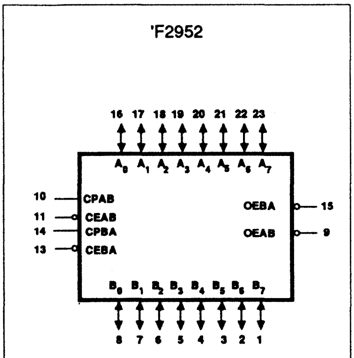
PIN CONFIGURATION DIP



PIN CONFIGURATION PLCC

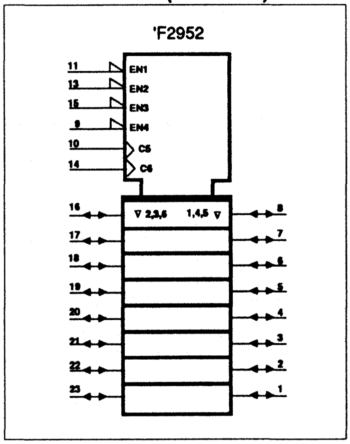


LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)



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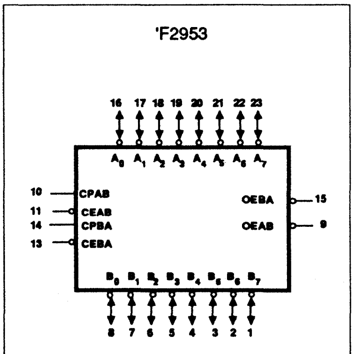
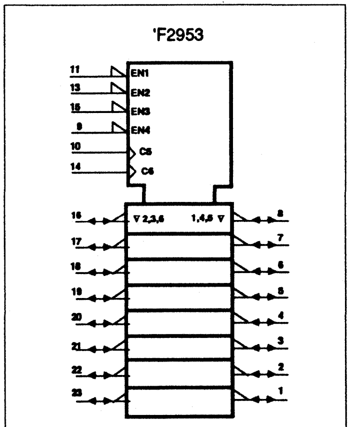


V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)



Document No.	853-0021
ECN No.	98774
Date of issue	February 9, 1990
Status	Product
FAST Products	

FAST 74F3037
30Ω Line Driver
Quad 2-Input NAND 30Ω Line Driver

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3037	2.0 ns	16 mA

FEATURES

- **30Ω line driver**
- **160mA output drive capability in the Low state**
- **67mA output drive capability in the High state**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**
- **Industrial temperature range available (-40°C to +85°C)**

DESCRIPTION

The 74F3037 is a high current Line Driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the 'F3037 is 67mA source and 160mA sink with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8V while driving impedances as low as 30 ohms. This is applicable with any combination of outputs using continuous duty.

The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performance may be improved by full or partial line termination.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
16-Pin Plastic DIP	N74F3037N	I74F3037N
16-Pin Plastic SOL[1]	N74F3037D	I74F3037D

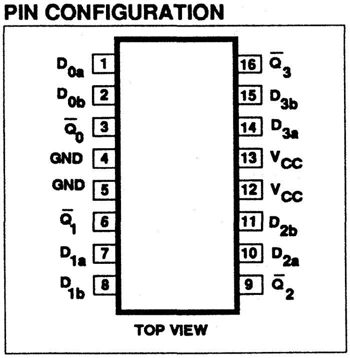
NOTE:
1. Thermal mounting techniques are recommended.
If driving impedances 42 ohms or greater then thermal mounting is not necessary.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

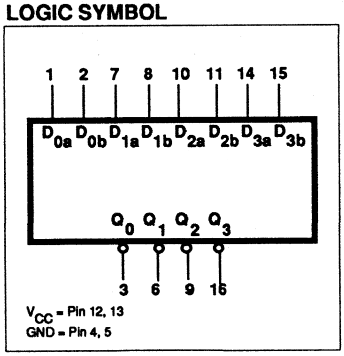
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_n$	Data outputs	3350/266	67mA/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

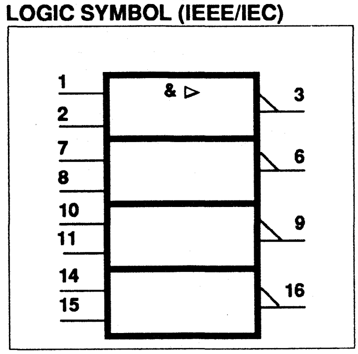
PIN CONFIGURATION



LOGIC SYMBOL

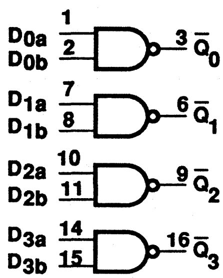


LOGIC SYMBOL (IEEE/IEC)



30Ω Line Driver FAST 74F3037

LOGIC DIAGRAM



V_{CC} = Pin 12, 13
GND = Pin 4, 5

FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	$\overline{Q}_n$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state		320	mA
T_A	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-67	mA
I_{OL}	Low-level output current				160	mA
T_A	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	-40		85	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

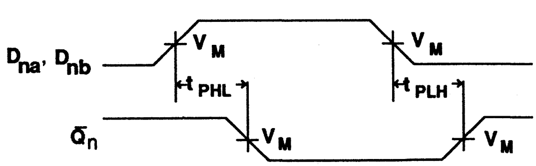
SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS Min	Typ[2]	Max	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -45mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH1} = -67mA[3]	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.30	0.50	V
			I_{OL1} = 160mA[4]	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_O	Output current[5]	V_{CC} = MAX, V_O = 2.25V			-100		-200	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX				6.0	9.0	mA
	I_{CCL}					30	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH1} is the current necessary to guarantee the Low to High transition in a 30 ohm transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30 ohm transmission line on the incident wave.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		T_A = -40°C to +85°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	1.0 1.0	2.0 2.0	5.0 4.5	1.0 1.0	5.5 5.0	1.0 1.0	5.5 5.0	ns

AC WAVEFORMS



Waveform 1. Propagation Delay for Inputs to Output

NOTE: For all waveforms, V_M = 1.5V.

Document No.	853-0022
ECN No.	98644
Date of issue	January 29, 1990
Status	Product
FAST Products	

FAST 74F3038
30Ω Line Driver

Quad Two-Input NAND 30Ω Line Driver (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3038	6.0 ns	17 mA

FEATURES

- **30Ω line driver**
- **160mA output drive capability**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	74F3038N
16-Pin Plastic SOL[1]	74F3038D

NOTE:
1. Thermal mounting techniques are recommended.
If driving impedances 42 ohms or greater then thermal mounting is not necessary.

DESCRIPTION

The 74F3038 is a high current Open- Collector Line Driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The 74F 3038 can sink 160mA with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OL} not more than 0.8V while driving impedances as low as 30 ohm. This is applicable with any combination of outputs using continuous duty.

The AC specifications for the 74F3038 were determined using the standard FAST load for open-collector parts of 50 pf capacitance, a 500 ohm pull-up resistor and a 500 ohm pull-down resistor. (See Test Circuit).

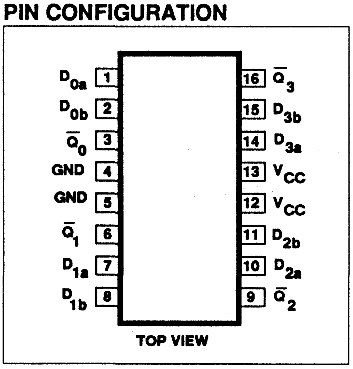
Reducing the load resistors to 100 ohm will decrease the t_{PLH} propagation delay by approximately 50 % while increasing t_{PHL} only slightly. The graph of typical propagation delay vs load resistor (See AC Characteristics section for Graph) shows a spline fit curve from four measured data points. R_L=30 ohm, R_L=100 ohm, R_L=300 ohm, and R_L=500 ohm.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

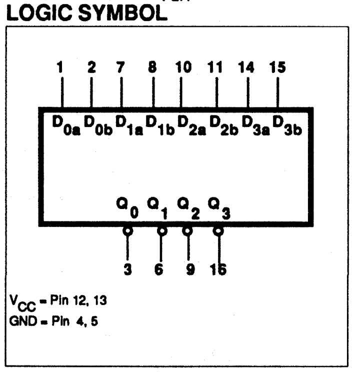
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_n$	Data outputs	OC/266	OC/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC = Open Collector

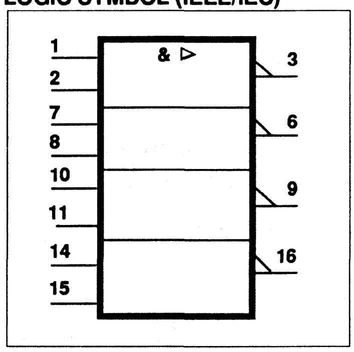
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



30Ω Line Driver FAST 74F3038

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

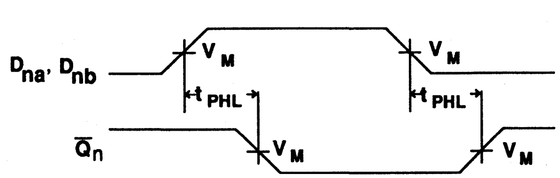
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	Typ[2]	Max	UNIT
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		.42	.55	V
				I_{OL} = 160mA[3]	±5%V_{CC}			.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{CC}	Supply current [total]	I_{CCH}	V_{CC} = MAX		V_{IN} =GND		3.5	6.0	mA
		I_{CCL}			V_{IN} = 4.5V		30	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	6.0 1.0	8.5 2.0	11.5 5.0	6.0 1.0	12.0 5.0	ns

AC WAVEFORMS



Waveform 1.Propagation Delay for Inputs to Output

NOTE: For all waveforms, V_M = 1.5V.

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Status	Product
FAST Products	

FAST 74F3040
30Ω Line Driver

Dual 4-Input NAND 30Ω Line Driver

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3040	2.0 ns	10 mA

FEATURES

- **30Ω line driver**
- **160mA output drive capability in the Low state**
- **67mA output drive capability in the High state**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

DESCRIPTION

The 74F3040 is a high current Line Driver composed of two 4-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the 'F3040 is 67mA source and 160mA sink with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8V while driving impedances as low as 30 ohms.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F3040N
16-Pin Plastic SOL[1]	N74F3040D

NOTE:
1. Thermal mounting techniques are recommended.
If driving impedances 42 ohms or greater then thermal mounting is not necessary.

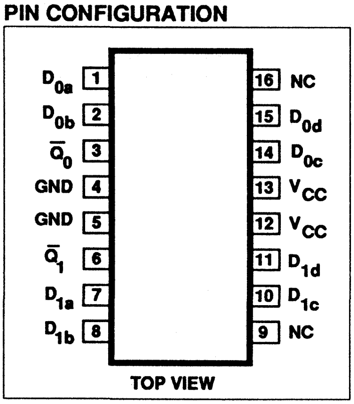
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_n$	Data output	3350/266	67mA/160mA

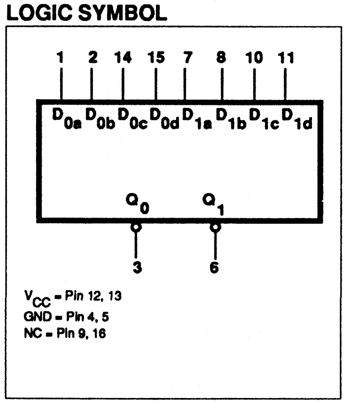
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

This is applicable with any combination of outputs using continuous duty.
The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices, Performance may be improved by full or partial line termination.

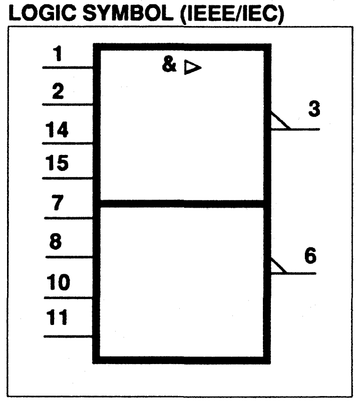
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



30Ω Line Driver FAST 74F3040

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

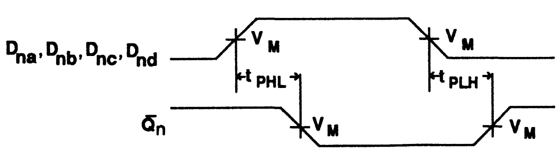
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	Typ[2]	Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -45mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH1} = -67mA[3]	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.30	0.50	V
				I_{OL1} = 160mA[4]	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_O	Output current[5]		V_{CC} = MAX, V_O = 2.25V			-100		-200	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				3.0	5.0	mA
		I_{CCL}					16	22	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH1} is the current necessary to guarantee the Low to High transition in a 30 ohm transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30 ohm transmission line on the incident wave.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to $\overline{Q}_n$	Waveform 1	1.0 1.0	2.0 2.0	5.0 4.5	1.0 1.0	5.5 5.0	ns

AC WAVEFORMS



Waveform 1. Propagation Delay for Inputs to Outputs

NOTE: For all waveforms, V_M = 1.5V.

Document No.	853-
ECN No.	
Date of issue	March 13, 1990
Status	Product Specification
FAST Products	

FAST 74F3893

Quad Futurebus Backplane Transceiver (3 State +Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3893	3.0ns	55mA

FEATURES

- **Quad Backplane Transceiver**
- **Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms**
- **Futurebus drivers sink 100mA**
- **Reduced voltage swing (1 volt) produces less noise and reduces power consumption**
- **High speed operation enhances performance of backplane buses and facilitates incident wave switching**
- **Compatible with IEEE 896 and IEEE 1194.1 Futurebus Standards**
- **Built-in precision band-gap (BG) reference provides accurate receiver threshold and improved noise immunity**
- **Glitch-free power up / power down operation on all outputs**
- **Pin and function compatible with NSC DS3893**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin PLCC	N74F3893A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/0.067	20µA/40µA
DE	Data Enable input	1.0/0.33	20µA/200µA
$\overline{RE}$	Receiver Enable input	1.0/0.067	20µA/40µA
I/O_0- I/O_3	Bus inputs	1.0/0.033	20µA/20µA
I/O_0- I/O_3	Bus outputs	OC/166.7	OC/100mA
R_0 - R_3	Receiver outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC = Open Collector

DESCRIPTION

The 74F3893 is a quad backplane transceiver and is intended to be used in very high speed bus systems.

The 74F3893 interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (< 5pF).

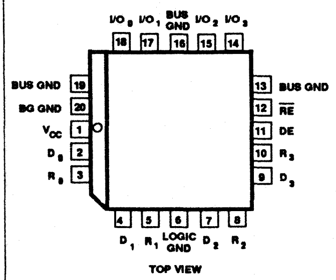
Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and short propagation delays. This results in a high bandwidth, reliable backplane.

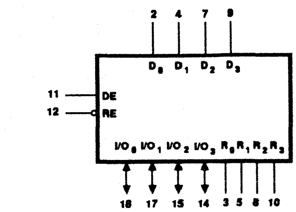
The 74F3893 has four TTL outputs (R_n) on the receiver side with a common Receive Enable input ($\overline{RE}$). It has four data inputs (D_n) which are also TTL. These data inputs are NANDed with the Data Enable input (DE). The four I/O pins (Bus side) are futurebus compatible, sink a minimum of 100mA, and are designed to drive heavily loaded backplanes with load impedances as low as 10 ohms. All outputs are designed to be glitch-free during power up and power down.

Quad Futurebus Backplane Transceiver FAST 74F3893

PIN CONFIGURATION

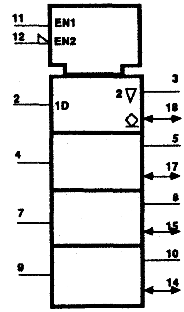


LOGIC SYMBOL

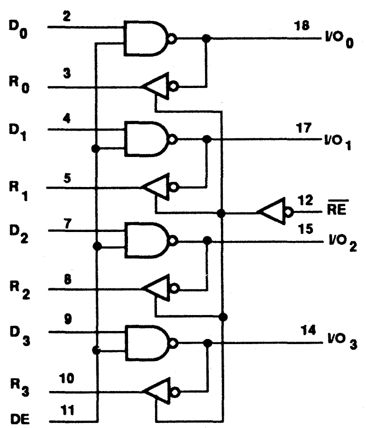


V_{CC} = Pin 1
LOGIC GND = Pin 6
BUS GND = Pin 13, 16, 19
BG GND = Pin 20

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 1
LOGIC GND = Pin 6
BUS GND = Pin 13, 16, 19
BG GND = Pin 20

FUNCTION TABLE

INPUTS			INPUT/OUTPUT	OUTPUT	OPERATING MODE
DE	$\overline{RE}$	D_n	I/O_n	R_n	
H H	L L	L H	H L	L H	Transmit to bus
H L	H H	D_n X	$\overline{D}_n$ H	Z Z	Receiver 3-state, Transmit to bus
L L	L L	X X	H L	L H	Receive, I/O_n =inputs

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-1.5 to +6.5	V
V_{IN}	Input voltage	-1.5 to +6.5	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	200	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS Min	Nom	Max	UNIT
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	D_n, DE, $\overline{RE}$	2.0			V
V_{IL}	Low-level input voltage	D_n, DE, $\overline{RE}$			0.8	V
I_{IK}	Input clamp current				-18	mA
V_{TH}	Bus input threshold	I/O_n only	1.475	1.55	1.625	V
I_{OH}	High-level output current	R_n only			-3	mA
I_{OL}	Low-level output current				100	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	Typ[2]	Max	UNIT
I_{OHB}	High-level output current	I/O_n	V_{CC}=MIN, V_{IL} = MAX, V_{IH} =MIN, V_{OH} = 1.5V			10	100	µA
V_{OH}	High-level output voltage	R_n	V_{CC} = MIN, V_{IL}= 1.3V, $\overline{RE}$ = 0.8V, I_{OH} = MAX		2.5			V
V_{OHB}	High-level output Bus voltage	I/O_n	V_{CC} = MAX , D_n = DE = 0.8V, V_T= 2.0V, R_T= 10Ω, $\overline{RE}$ =2.0V		1.9			V
V_{OL}	Low-level output voltage	R_n	V_{CC} = MIN, V_{IN} = 1.8V, $\overline{RE}$=0.8V, I_{OL} = 6mA			0.35	0.5	V
V_{OLB}	Low-level output Bus voltage	I/O_n	D_n = DE = V_{IH}, I_{OL}= 100mA		0.75	1.0	1.2	V
			D_n = DE = V_{IH}, I_{OL}= 80mA		0.75	1.0	1.1	V
V_{OCB}	Driver output positive clamp voltage	I/O_n	V_{CC} = MAX or 0V, I/O_n =1mA	D_n = DE = 0.8V	1.9		2.9	V
			V_{CC} = MAX or 0V, I/O_n =10mA	$\overline{RE}$ = 2.0V	2.3		3.2	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V, DE = $\overline{RE}$ = D_n = V_{CC}				100	µA
I_{IH}	High-level input current	D_n , $\overline{RE}$, DE	V_{CC} = MAX, DE = $\overline{RE}$ = D_n = 5.5V				20	µA
I_{IHB}	High-level I/O bus current (power off)	I/O_n	V_{CC} = 0V, D_n = DE = 0.8V, I/O_n = 1.2V, $\overline{RE}$ = 0V				100	µA
I_{IL}	Low-level input current	D_n , $\overline{RE}$	V_{CC} = MAX, V_I = 0.5V, DE = 4.5V				-40	µA
		DE	V_{CC} = MAX, V_I = 0.5V, D_n = 4.5V				-200	µA
I_{ILB}	Low-level I/O bus current (power on)	I/O_n	V_{CC} = MAX, D_n = DE = 0.8V, I/O_n = 0.75V, $\overline{RE}$ = 0V		-20		20	µA
I_{OZH}	Off-state output current, High-level voltage applied	R_n	V_{CC} = MAX, V_O =2.7V, $\overline{RE}$=2V				20	µA
I_{OZL}	Off-state output current, Low-level voltage applied	R_n	V_{CC} = MAX, V_O =0.5V, $\overline{RE}$=2V				-20	µA
I_{OS}	Short-circuit output current[3]	R_n	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, ($\overline{RE}$ =V_{IH} or V_{IL})			55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for Driver and Driver Enable

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $V_T = 2V$, $C_D = 50pF$, $R_T = 10\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $V_T = 2V$, $C_D = 50pF$, $R_T = 10\Omega$		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to I/O_n	Waveform 1	1.0 1.5	2.0 3.0	5.0 5.5	1.0 1.5	5.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay DE to I/O_n	Waveform 1	1.0 1.5	2.0 3.0	4.5 5.5	1.0 1.5	5.5 6.0	ns
t_{TLH} t_{THL}	D_n to I/O_n Transition time 10% to 90%, 90% to 10%	Waveform 1	1.0 1.0		4.0 4.0	1.0 1.0	5.0 5.0	ns
t_{Dskew}	Skew between Drivers in same package			1.0				ns

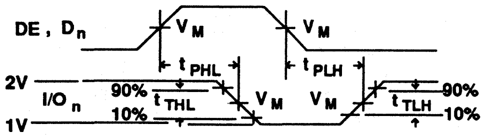
AC ELECTRICAL CHARACTERISTICS for Receiver

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 1k\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 1k\Omega$		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I/O_n to R_n	Waveform 2	1.0 3.6	2.0 5.5	4.5 7.75	1.0 3.6	5.5 8.5	ns

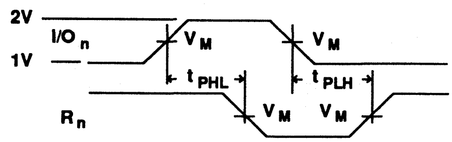
AC ELECTRICAL CHARACTERISTICS for Receiver Enable

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
t_{PZH} t_{PZL}	Output Enable to High or Low level $\overline{RE}$ to R_n	Waveform 3 Waveform 4	1.5 2.5	3.0 4.0	5.5 7.0	1.5 2.0	6.0 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable from High or Low level $\overline{RE}$ to R_n	Waveform 3 Waveform 4	1.5 1.5	3.0 3.0	5.5 5.5	1.0 1.0	6.5 6.0	ns

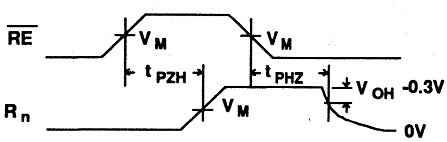
AC WAVEFORMS



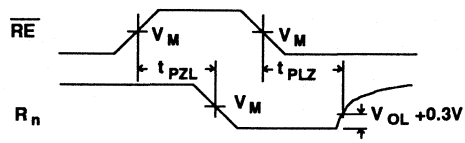
Waveform 1. Propagation Delay For Driver



Waveform 2. Propagation Delay For Receiver



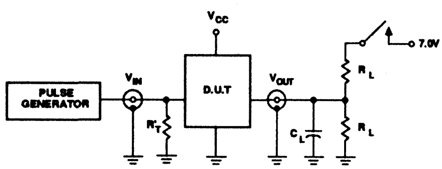
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

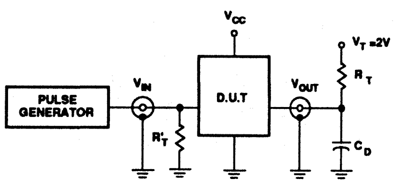
TEST CIRCUIT AND WAVEFORMS



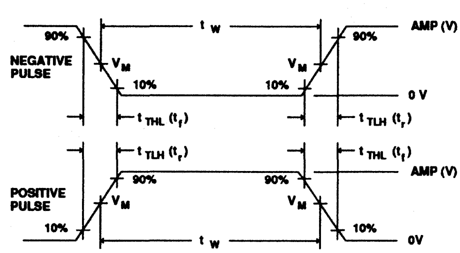
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit For Open Collector Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	**Rep. Rate**	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R'_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistor; see AC CHARACTERISTICS for value.

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FAST Products	

FAST 74F5074 Flip-Flop/ Clock Driver

Synchronizing Dual D-Type Flip-Flop With Metastable Immune Characteristics

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F5074	120 MHz	20mA

FEATURES

- **Metastable Immune Characteristics**
- **Propagation delay skew and output to output skew guaranteed less than 1.5ns**
- **High source current (I_{OH} = 15mA) ideal for clock driver applications**
- **Pinout compatible with 74F74**
- **See 74F50728 for Synchronizing Cascaded D-Type Flip-Flop**
- **See 74F50729 for Synchronizing Dual D-Type Flip-Flop with Edge-Triggered Set and Reset**
- **See 74F50109 for Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flops**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F5074N
14-Pin Plastic SO	N74F5074D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

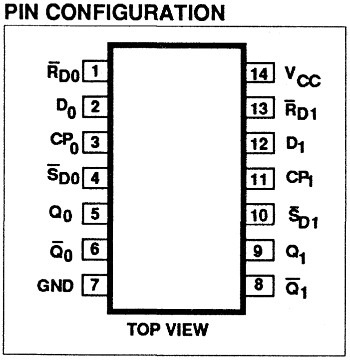
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/0.417	20µA/250µA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.033	20µA/20µA
$\overline{S}_{D0}$, $\overline{S}_{DI}$	Set inputs (active Low)	1.0/0.033	20µA/20µA
$\overline{R}_{D0}$, $\overline{R}_{DI}$	Reset inputs (active Low)	1.0/0.033	20µA/20µA
Q_0, Q_I, $\overline{Q}_0$, $\overline{Q}_I$	Data outputs	750/33	15mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

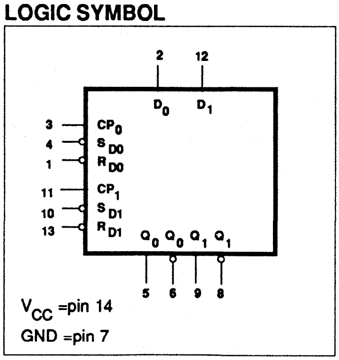
DESCRIPTION

The 74F5074 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.
Set ($\overline{S}_{Dn}$) and Reset ($\overline{R}_{Dn}$) are asynchronous active-Low inputs and operate independently of the Clock (CP_n) input. Data must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays.
Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D_n input may be changed without affecting the levels of the output.
The 74F5074 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F5074 are: $\tau \cong$ 135ps and $T_0 \cong 9.8 \times 10^6$ sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state.

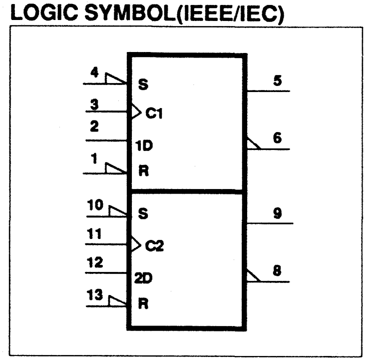
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Metastable Immune Characteristics

Signetics uses the term 'metastable immune' to describe characteristics of some of the products in its FAST family. Specifically the 74F50XXX family presently consists of 4 products which display metastable immune characteristics. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations. This claim is easily verified on the 74F5074.

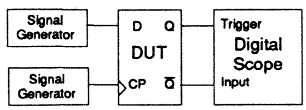


Fig. 1—Test Set up

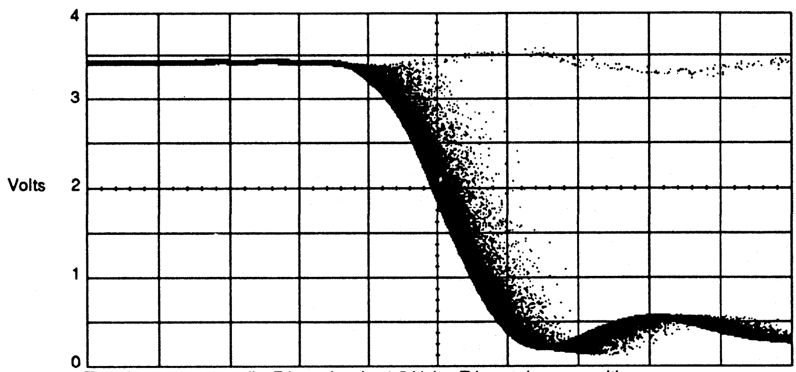
By running two independent signal generators (see Fig. 1) at nearly the same frequency (in this case 10 MHz clock and 10.02 MHz data) the device-under-test can often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

When the device-under-test is a 74F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Fig. 2.

Fig. 2 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5 volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output
did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

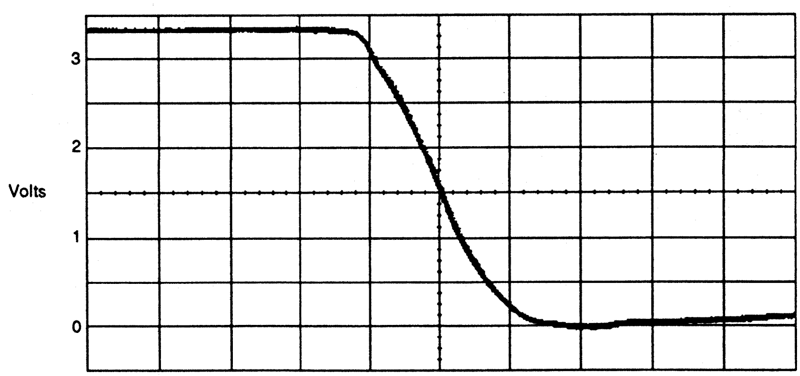
When the device-under-test is a metastable immune part, such as the 74F5074, the waveform will appear as in Fig. 3. The 74F5074 $\overline{Q}$ output will not vary with respect to the Q trigger point even when the part is driven into a metastable state. Any tendency towards internal metastability is resolved by Signetics

COMPARISON OF METASTABLE IMMUNE AND NON-IMMUNE CHARACTERISTICS



Time base = 2.00ns/div Trigger level = 1.5 Volts Trigger slope = positive

Fig. 2—74F74 $\overline{Q}$ output triggered by Q output, setup and hold times violated



Time base = 2.00ns/div Trigger level = 1.5 Volts Trigger slope = positive

Fig. 3—74F5074 $\overline{Q}$ output triggered by Q output, setup and hold times violated

patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased Clock-to-Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the part defined by τ and T_o.

The metastability characteristics of the 74F5074 and related part types represent state-of-the art in TTL technology.
After determining the T_o and τ of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the F5074 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz , and has decided that he would like to sample the output of the F5074 10 nanoseconds after the clock edge.
He simply plugs his numbers into the equation below:

$$MTBF = e^{(t'/\tau)} / T_o f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t'>h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency or 20MHz because input events consist of both low and high data transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Fig. 4 it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula the actual MTBF is 1.51 x 10^{10} seconds or about 480 years.

MEAN TIME BETWEEN FAILURES (MTBF) versus t'

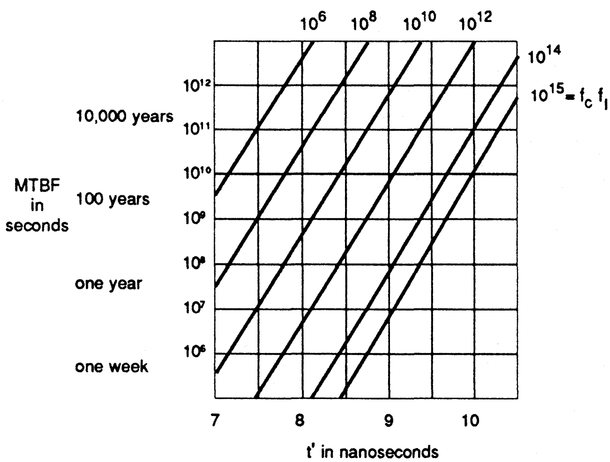
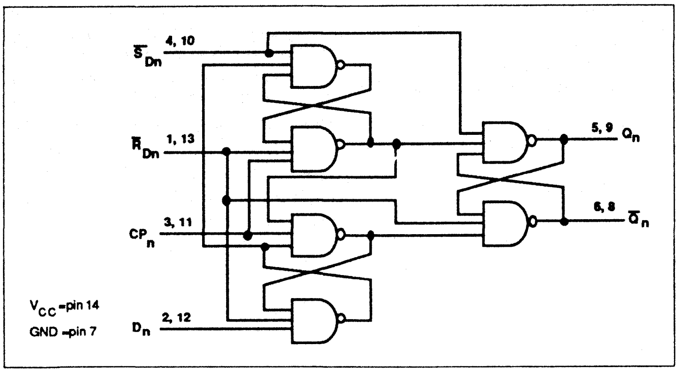


Fig. 4 MTBF versus t' for 74F5074 at τ = 135ps and T_o=9.8x 10^6 sec

Typical values for τ and T_o at various V_{CC}s and Temperatures

	0°C		25°C		70°C	
	τ	T_o	τ	T_o	τ	T_o
5.5 V	125 ps	1.0 x 10^9 sec	138ps	5.4 x 10^6sec	160 ps	1.7 x 10^5sec
5.0 V	115ps	1.3 x 10^{10} sec	135 ps	9.8 x 10^6sec	167ps	3.9 x 10^4sec
4.5 V	115 ps	3.4 x 10^{13}sec	132ps	5.1 x 10^8sec	175 ps	7.3 x 10^4sec

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{S}_{Dn}$	$\overline{R}_{Dn}$	CP_n	D_n	Q_n	$\overline{Q}_n$	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↑̸	X	NC	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
NC = No change from the previous setup
X = Don't care
↑ = Low-to-High clock transition
↑̸ = Not a Low-to-High clock transition
* = This setup is unstable and will change when either Set or Reset return to the High level.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS Min	LIMITS Nom	LIMITS Max	UNIT
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$V_{CC}\pm10\%$			-12	mA
		$V_{CC}\pm5\%$			-15	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -12mA	$\pm10\%V_{CC}$	2.5			V
					$\pm5\%V_{CC}$	2.7	3.4		V
				I_{OH} = -15mA	$\pm5\%V_{CC}$	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	$\pm10\%V_{CC}$		0.30	0.50	V
					$\pm5\%V_{CC}$		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	D_n	V_{CC} = MAX, V_I = 0.5V					-250	µA
		$CP_n, \overline{S}_{Dn}, \overline{R}_{Dn}$						-20	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				20	30	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

AC ELECTRICAL CHARACTERISTICS

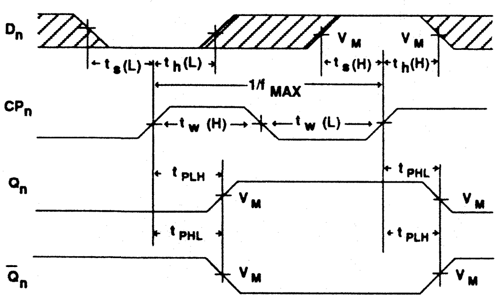
SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	120		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	3.9 3.9	6.0 6.0	1.5 2.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	3.0 3.0	4.5 5.0	7.5 7.5	2.5 2.5	8.0 8.0	ns
t_{PS}	Propagation delay Skew[1,3]	Waveform 4			1.0		1.0	ns
t_{OS}	Output to output Skew[2,3]	Waveform 4			1.5		1.5	ns

NOTE:
1. $\mid t_{PLH}$ actual - t_{PHL} actual $\mid$ for any output.
2. $\mid t_{PN}$ actual - t_{PM} actual $\mid$ for any output compared to any other output where N and M are either LH or HL.
3. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

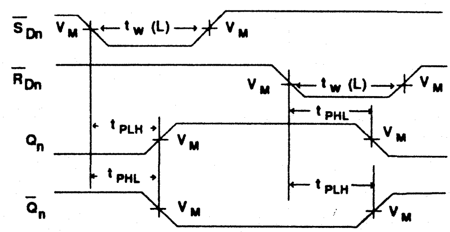
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP_n	Waveform 1	1.5 1.5			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP_n	Waveform 1	1.0 1.0			1.5 1.5		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 4.0			3.0 4.5		ns
$t_w(L)$	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ Pulse width, Low	Waveform 2	3.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to CP_n	Waveform 3	3.0			3.5		ns

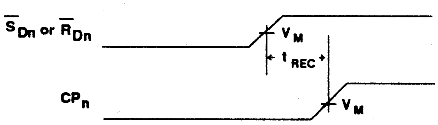
AC WAVEFORMS



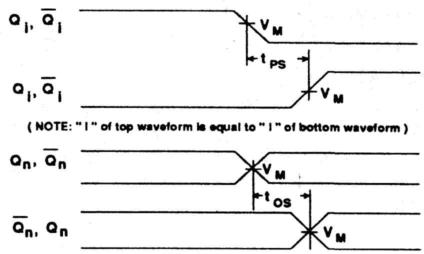
Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width



Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width



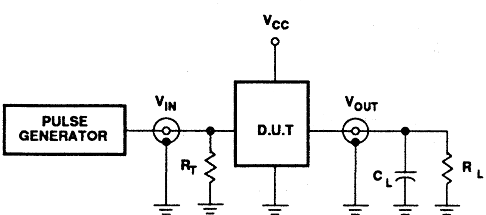
Waveform 3.
Recovery time for set or reset to clock



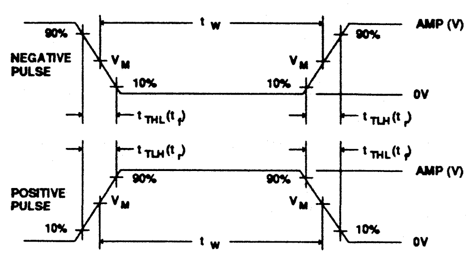
Waveform 4.
Propagation delay skew and output to output skew

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Document No.	853-1409
ECN No.	98304
Date of issue	December 13, 1989
Status	Product Specification
FAST Products	

FAST 74F5300
Fiber Optic LED Driver

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F5300	2.5 ns	8.0mA

FEATURES
- TTL inputs
- Output enable control
- High current source and sink capability
- Matched propagation delay times (t_{PLH}, t_{PHL})
- Symmetrical rise and fall times
- ESD protection greater than 2000 volts
- Single +5V supply
- Surface mount package

APPLICATIONS
- High speed serial data communication
- Fiber optic data links
- Local area and metropolitan area networks
- Digital Television
- PBX systems

ASSOCIATED PRODUCTS
- NE 5210/11/12 transimpedance amplifiers
- NE5214/5217 postamplifiers with link status indicator
- 74F5302 dual fiber optic LED driver

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V\pm10\%$; $T_A = 0°C$ to $+70°C$
8-Pin Plastic DIP	74F5300N
8-Pin Plastic SO	74F5300D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Input	Data input	1.0/1.0	20μA/0.6mA
Enable	Enable input	1.0/1.0	20μA/0.6mA
Output	Current driver output	8000/266.6	160mA/160mA

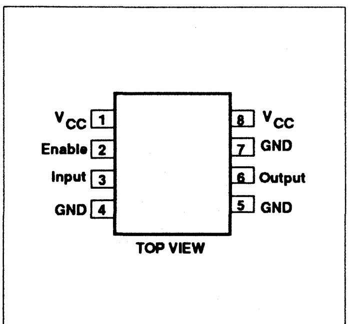
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

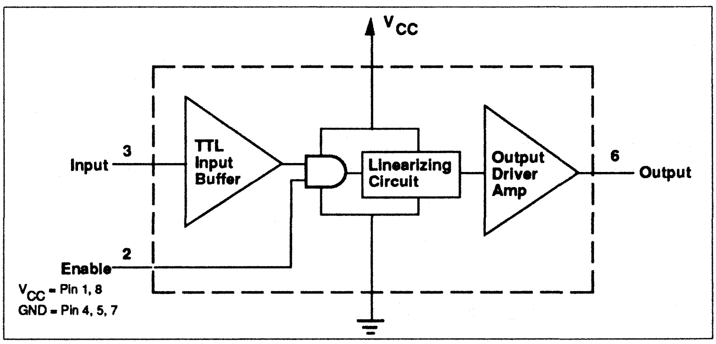
The 74F5300 is a LED driver designed for use in fiber optics links. The 74F5300 is ideally suited for use in high speed optical high transmitter systems.

The TTL input buffer accepts TTL data. A logic High on the Enable pin enables the buffer to drive the output driver amplifier.The Linearizing Circuit ensures a constant propagation delay for t_{PLH} and t_{PHL}, and controls the rise and fall times.The output driver amplifier is capable of sourcing more than 160 mA and sinking more than 160 mA at low impedances. The high current output driver has been designed to deal with transmission line effects of high speed switching systems with fast rising and falling edges.The performance of the system can be enhanced by matching impedance at the output for proper termination.It exhibits closely matched propagation delays

PIN CONFIGURATION



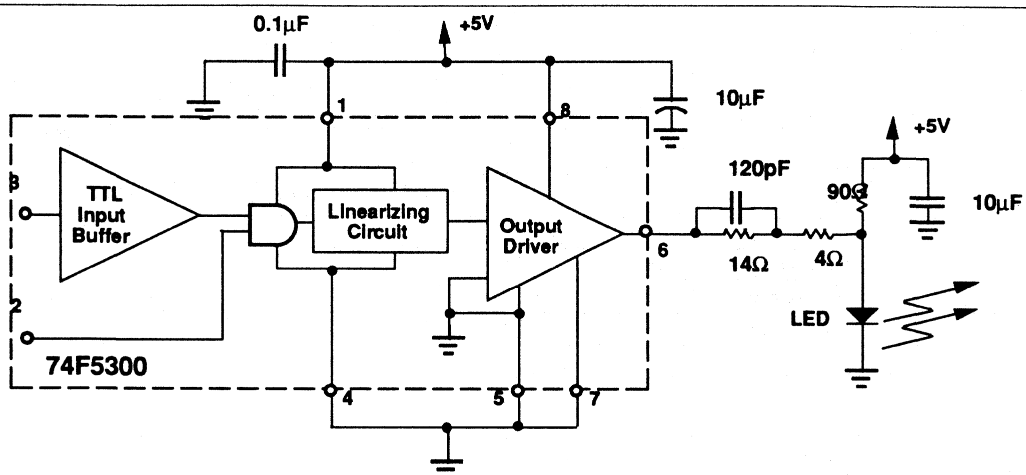
LOGIC DIAGRAM



(t_{PHL}, t_{PLH}) and symmetrical rise and fall times. The resulting optical waveform has minimal Duty Cycle Distortion (DCD). When used with the external pre-bias and pre-charging circuits, the response can be tailored to a specific LED to eliminate any overshoot and to minimize the long fall response.

Additionally, this part can be used as the transmiter in a complete fiber optic system when combined with any of the NE5210/5211/5212 preamplifiers and NE5214/5217 preamplifiers for the optical receiver. Please refer to applications note AN1121 in the Signetics Fiber Optic Communication Data Book for more specific applications information.

APPLICATION



50Mb/s Optical Transmitter

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	240	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-160	mA
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS Min	Typ[2]	Max	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}= -80mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.8	3.3	3.9	V
				V_{CC} = 5V	3.0	3.3	3.6	V
			I_{OH}= -160mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}= 100mA	±10%V_{CC}		0.42	0.55	V
			I_{OL}= 120mA	±10%V_{CC}		0.45	0.60	V
			I_{OL}= 160mA	±10%V_{CC}		0.55	0.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX				4.0	12	mA
	Supply current (total) I_{CCL}					10.5	22	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The device is not short circuit protected.

AC ELECTRICAL CHARACTERISTICS

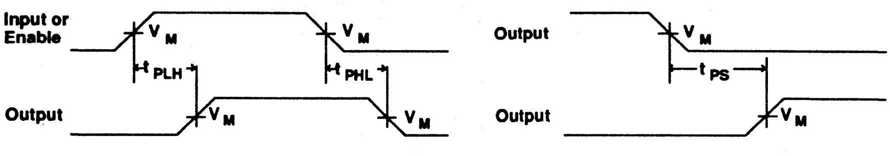
SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 100Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 100Ω		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Input or Enable to Output	Waveform 1	1.0 1.0	2.5 2.5	5.0 5.0	1.0 1.0	5.0 5.0	ns
D_{tpw}	Pulse width distortion[1]	Frequency = 10MHz		0.8	1.2		1.8	ns
t_{PS}	Propagation delay Skew[2,4]	Waveform 2		0.7	1.2		1.3	ns
t_{RFS}	Rise and Fall time Skew[3,4]			0.6	1.5		1.5	ns
t_{THL} t_{TLH}	Fall time 90% to 10% Rise time 10% to 90%	Test circuits and Waveforms	0.5 1.0	1.4 2.0	3.5 4.0	0.5 1.0	4.0 4.5	ns

NOTE:
1. D_{tpw} is defined as the difference between input pulse width and output pulse width (0 to 3 volt input swing and 50% duty cycle).
2. | t_{PLH} actual - t_{PHL} actual | .
3. | t_{TLH} actual - t_{THL} actual | .
4. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

Fiber Optic LED Driver

FAST 74F5300

AC WAVEFORMS

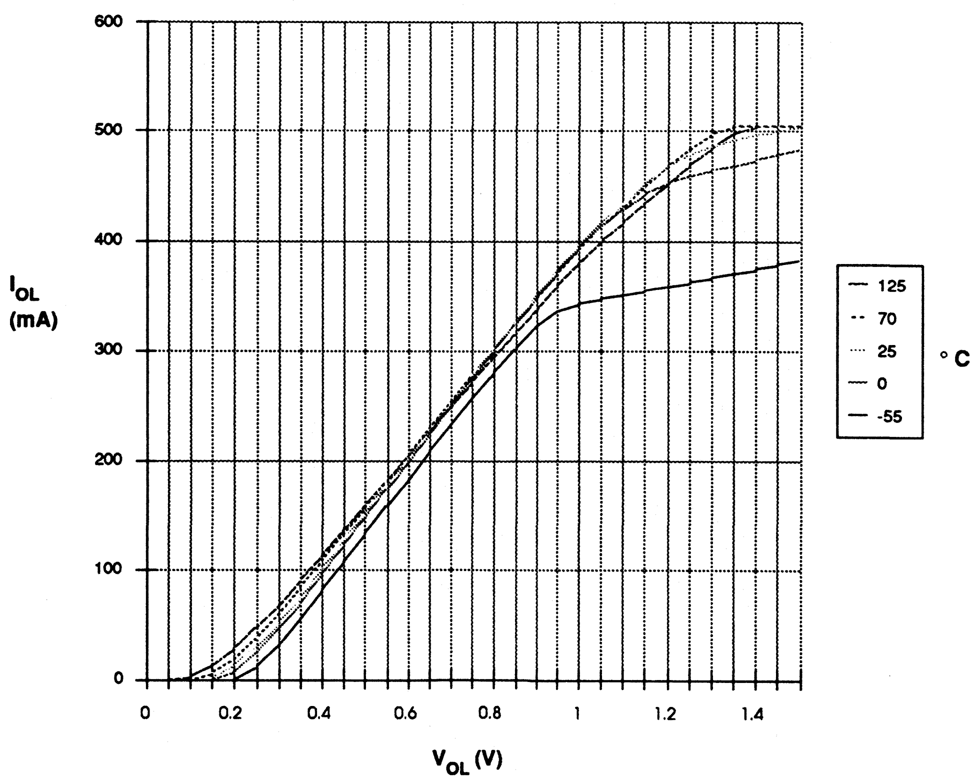


Waveform 1. Propagation Delay for Input to Output

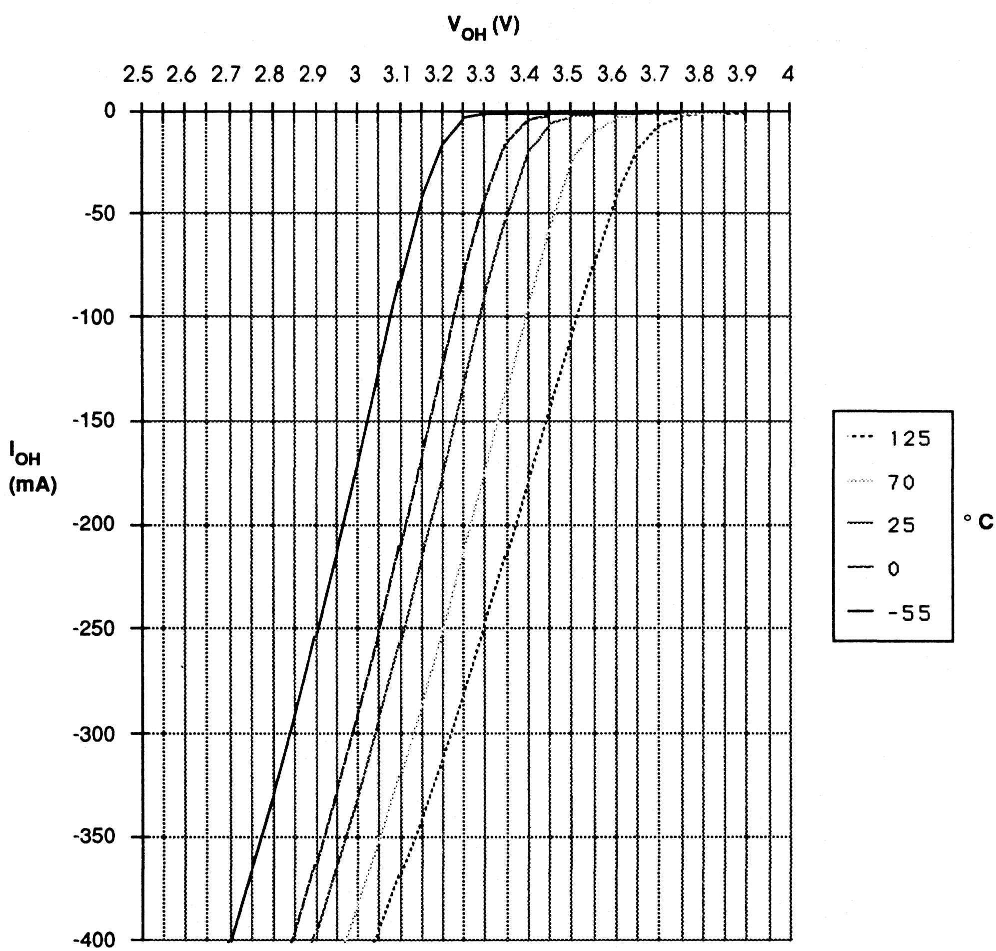
Waveform 2. Propagation Delay Skew

NOTE: For all waveforms, $V_M = 1.5V$.

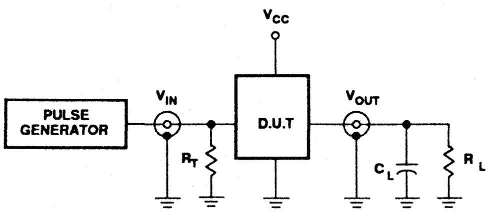
TYPICAL (V_{CC} =5.0V) V_{OL} VERSUS I_{OL} FOR VARIOUS TEMPERATURES



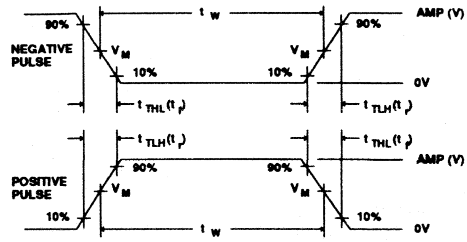
TYPICAL (V_{CC} =5.0V) V_{OH} VERSUS I_{OH} FOR VARIOUS TEMPERATURES



TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-1410
ECN No.	98485
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F5302

Fiber Optic Dual LED /Clock Driver

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F5302	2.5 ns	8.0mA

FEATURES

- **TTL inputs**
- **Output enable control**
- **High current source and sink capability**
- **Matched propagation delay times (t_{PLH}, t_{PHL})**
- **Symmetrical rise and fall times**
- **ESD protection greater than 2000 volts**
- **Single +5V supply**
- **Surface mount package**

APPLICATIONS

- **High speed serial data communication**
- **Fiber optic data links**
- **Local area and metropolitan area networks**
- **Digital Television**
- **PBX systems**

ASSOCIATED PRODUCTS

- **NE 5210/11/12 transimpedance amplifiers**
- **NE5214/5217 postamplifiers with link status indicator**
- **74F5300 fiber optic LED driver**

DESCRIPTION

The 74F5302 is a dual LED/ Clock driver designed for use in fiber optics links. The 74F5302 is ideally suited for use in high speed optical high transmitter systems. It is also ideal for use as a clock driver.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	74F5302N
14-Pin Plastic SO	74F5302D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20µA/0.6mA
Q_n	Current driver outputs	8000/266.6	160mA/160mA

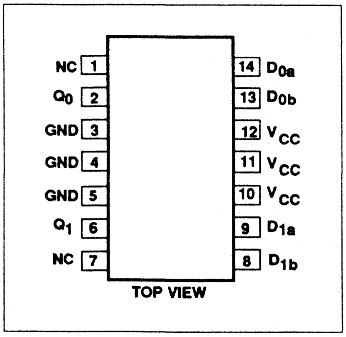
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

The TTL input buffer accepts TTL data. The Linearizing Circuit ensures a constant propagation delay for t_{PLH} and t_{PHL}, and controls the rise and fall times. The output driver amplifier is capable of sourcing more than 160 mA and sinking more than 160 mA at low impedances. The high current output driver has been designed to deal with transmission line effects of high speed switching systems with fast rising and falling edges. The performance of the system can be enhanced by matching impedance at the output for proper termination. It exhibits closely matched propagation delays (t_{PHL}, t_{PLH}) and symmetrical rise and fall times. The resulting optical waveform has minimal Duty Cycle Distortion (DCD). When used with the external pre-bias and pre-charging circuits, the response can be tailored to a specific LED to eliminate any overshoot and to minimize the long fall response.

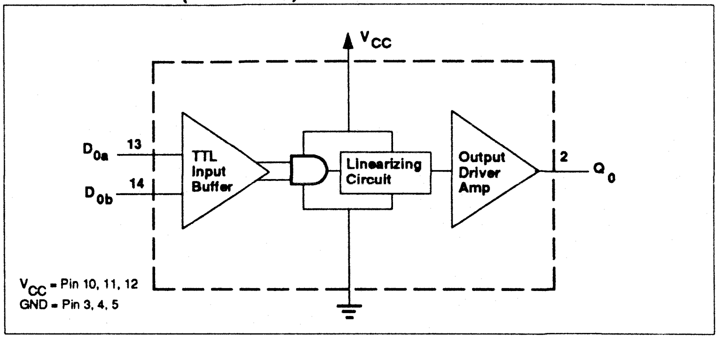
Additionally, this part can be used as the transmiter in a complete fiber optic system when combined with any of the NE5210/5211/5212 preamplifiers and NE5214/5217 preamplifiers for the optical receiver. Please refer to applications note AN1121 in the Signetics Fiber Optic Communication Data Book for more specific applications information.

Fiber Optic LED Driver FAST 74F5302

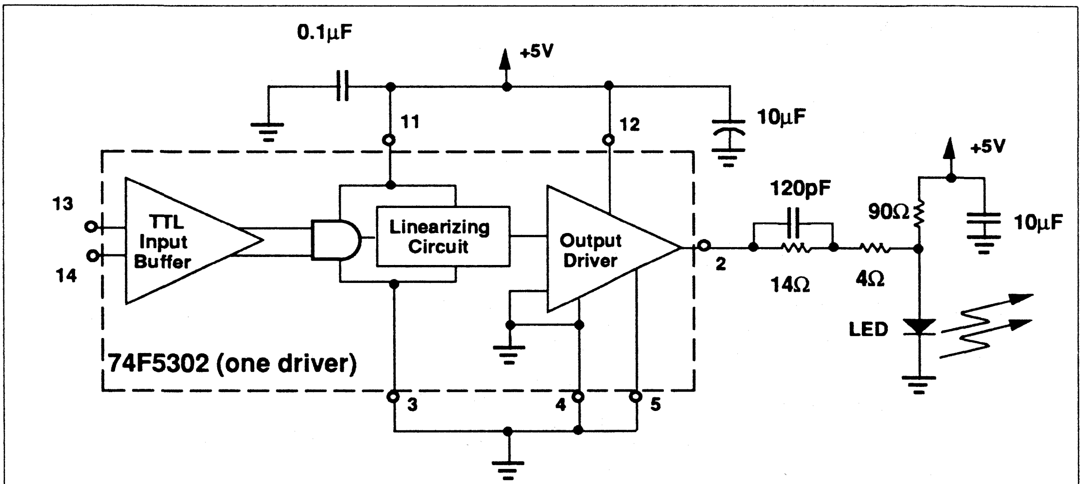
PIN CONFIGURATION



LOGIC DIAGRAM (One driver)



APPLICATION



50Mb/s Optical Transmitter

Fiber Optic LED Driver FAST 74F5302

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	240	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS Min	LIMITS Nom	LIMITS Max	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-160	mA
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}= -80mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.8	3.3	3.9	V
				V_{CC} = 5V	3.0	3.3	3.6	V
			I_{OH}= -160mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}= 100mA	±10%V_{CC}		0.42	0.55	V
			I_{OL}= 120mA	±10%V_{CC}		0.45	0.60	V
			I_{OL}= 160mA	±10%V_{CC}		0.55	0.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX				5.0	12	mA
	I_{CCL}					18	25	mA

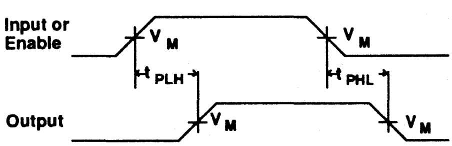
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The device is not short circuit protected.

AC ELECTRICAL CHARACTERISTICS

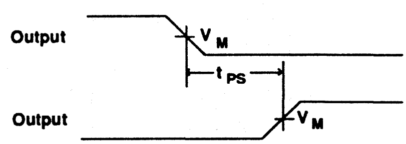
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 100\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 100\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	Waveform 1	1.0 1.0	2.0 2.5	4.5 5.0	1.0 1.0	4.5 5.0	ns
D_{tpw}	Pulse width distortion[1]	Frequency = 10MHz		0.8	1.2		1.8	ns
t_{PS}	Propagation delay Skew[2,4]	Waveform 2		0.8	1.2		1.3	ns
t_{RFS}	Rise and Fall time Skew[3,4]			0.3	1.5		2.0	ns
t_{OS}	Output to output Skew[4]			0.9	1.3		1.6	ns
t_{THL} t_{TLH}	Fall time 90% to 10% Rise time 10% to 90%	Test circuits and Waveforms	1,0 1.0	1.5 1.8	3.0 3.0	0.5 0.5	4.0 4.5	ns

NOTES:
1. D_{tpw} is defined as the difference between input pulse width and output pulse width (0 to 3 volt input swing and 50% duty cycle).
2. $| t_{PLH}$ actual - t_{PHL} actual $|$.
3. $| t_{TLH}$ actual - t_{THL} actual $|$.
4. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS



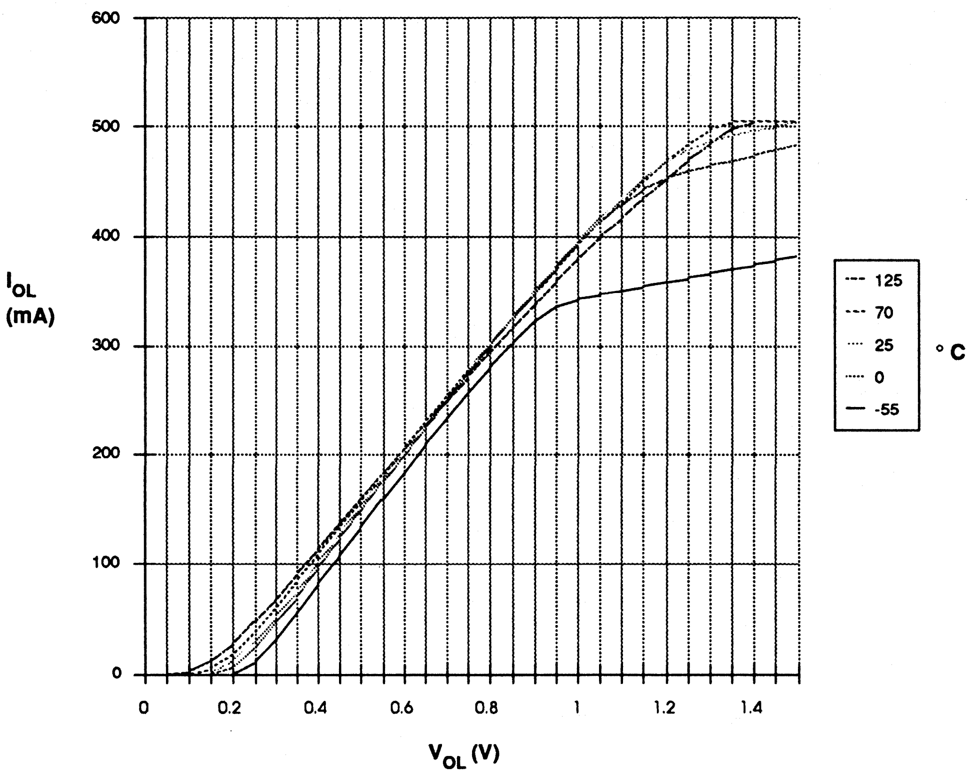
Waveform 1. Propagation Delay for Input to Output



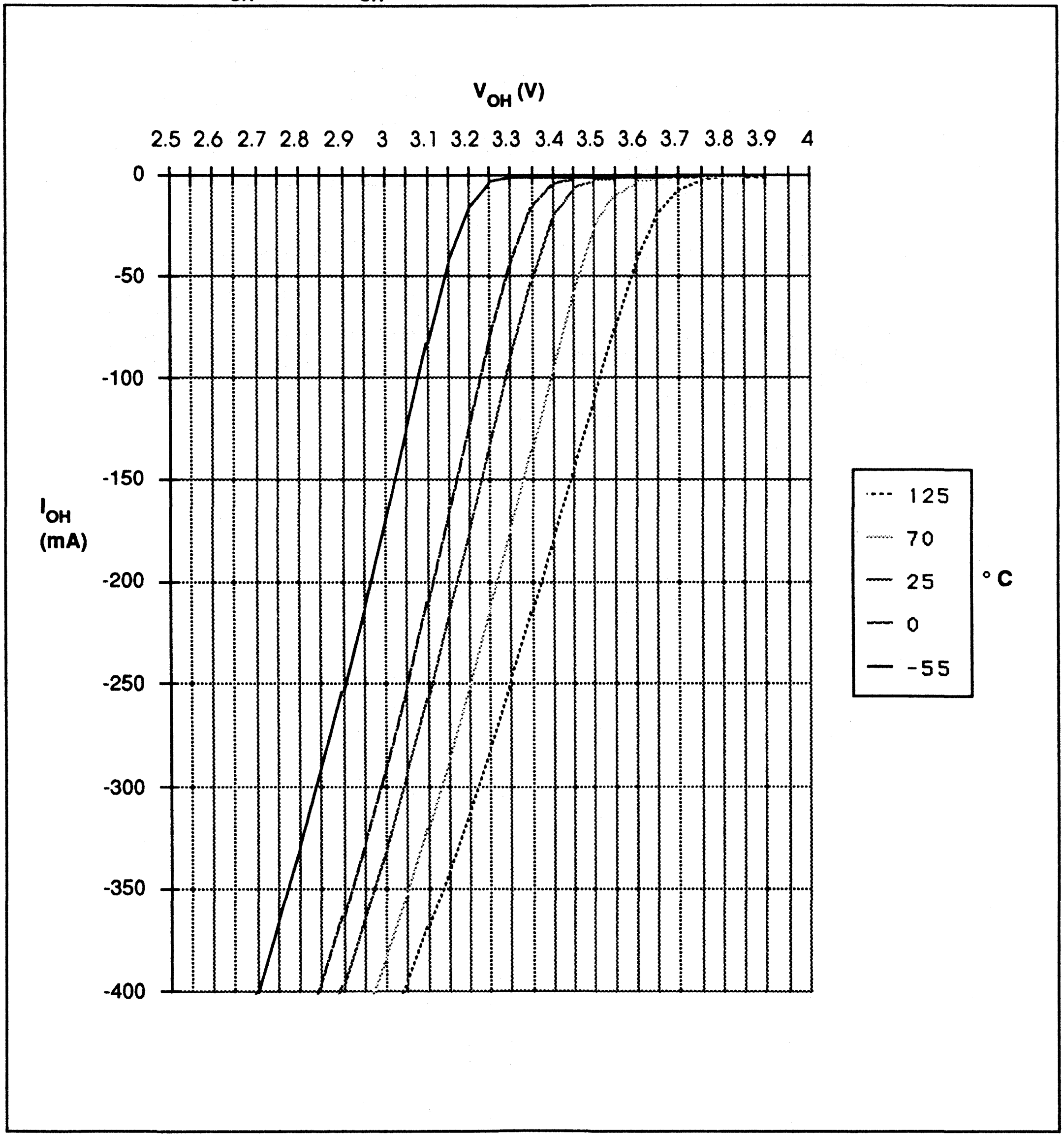
Waveform 2. Propagation Delay Skew

NOTE: For all waveforms, $V_M = 1.5V$.

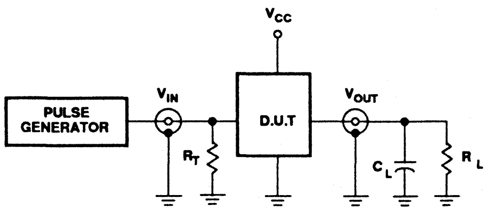
TYPICAL (V_{CC} =5.0V) V_{OL} VERSUS I_{OL} FOR VARIOUS TEMPERATURES



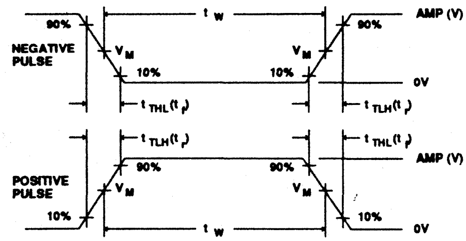
TYPICAL (V_{CC} =5.0V) V_{OH} VERSUS I_{OH} FOR VARIOUS TEMPERATURES



TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-1120
ECN No.	
Date of issue	June 12, 1990
Status	Product Specification
FAST Products	

FAST 74F8960, 74F8961

Futurebus Transceivers

74F8960-Octal Latched Bidirectional Futurebus Transceiver, INV (OC)
74F8961-Octal Latched Bidirectional Futurebus Transceiver, NINV (OC)

FEATURES

- **Octal Latched Transceiver**
- **Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms**
- **High drive (100mA) open collector drivers on B-port**
- **Reduced voltage swing (1 volt) produces less noise and reduces power consumption**
- **High speed operation enhances performance of backplane buses and facilitates incident wave switching**
- **Compatible with IEEE 896 Futurebus Standard**
- **Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity**
- **Controlled output ramp and multiple GND pins minimize ground bounce**
- **Glitch-free power up / power down operation**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F8960	6.5ns	80mA
74F8961	6.5ns	80mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (600 mil)[1]	N74F8960N, N74F8961N
28-Pin PLCC[1]	N74F8960A, N74F8961A

NOTE:
1. Thermal mounting techniques are recommended.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	PNP latched inputs	3.5/0.0117	70µA/70µA
B_0 - B_7	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA	A Output Enable input (active High)	1.0/0.033	20µA/20µA
$\overline{OEB}_0$, $\overline{OEB}_1$	B Output Enable inputs (active Low)	1.0//0.033	20µA/20µA
$\overline{LE}$	Latch Enable input (active Low)	1.0//0.033	20µA/20µA
A_0 - A_7	3-State outputs	150/40	3mA/24mA
B_0 - B_7	Open Collector outputs	OC*/166.7	OC*/100mA

NOTES:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
* OC = Open Collector

DESCRIPTION

The 74F8960 and 74F8961 are octal bidirectional latched transceivers and are intended to provide the electrical interface to a high performance wired-OR bus. The B port inverting drivers are low-capacitance open collector with controlled ramp and are designed to sink 100 mA from 2 volts. The B port receivers have a 100 mV threshold region and a 4 ns glitch filter.

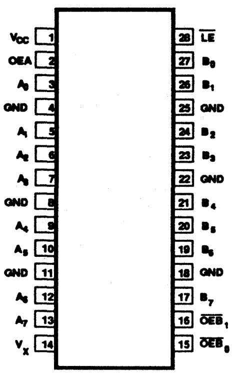
The B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (<5 pF).

Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.
BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.
The 74F8960 and 74F8961 A ports have TTL 3-State drivers and TTL receivers with a latch function. A separate High level control input (V_X) is provided to limit the A port output level to a given voltage level (such as 3.3V). For 5.0V systems, V_x is simply tied to V_{CC}.

74F8961 is the non-inverting version of 74F8960.

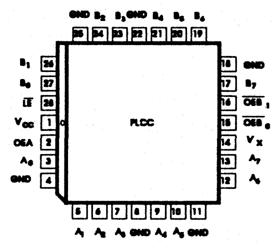
PIN CONFIGURATION DIP

74F8960



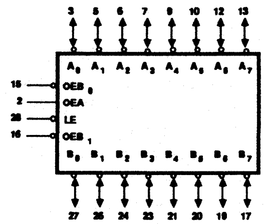
PIN CONFIGURATION PLCC

74F8960



LOGIC SYMBOL

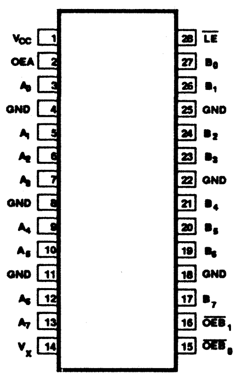
74F8960



V_{CC} = Pin 1 V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

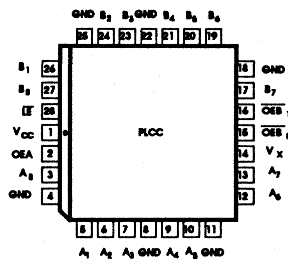
PIN CONFIGURATION

74F8961



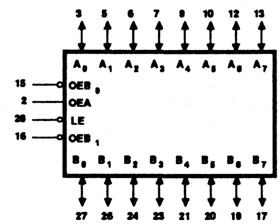
PIN CONFIGURATION PLCC

74F8961



LOGIC SYMBOL

74F8961

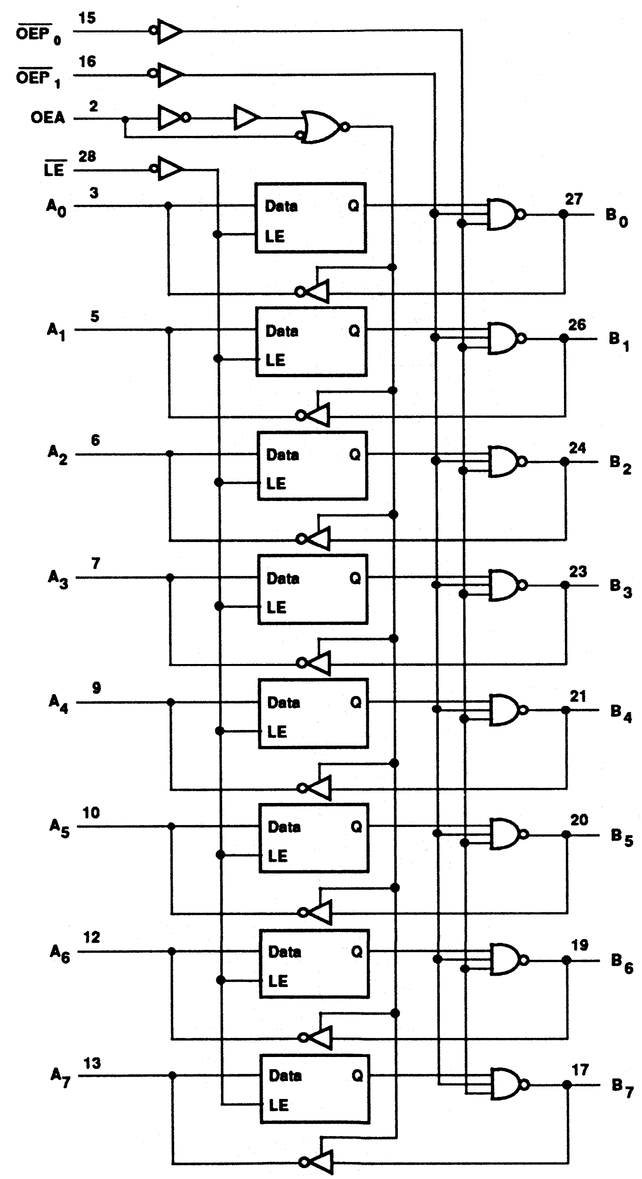


V_{CC} = Pin 1 V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

PIN DESCRIPTION

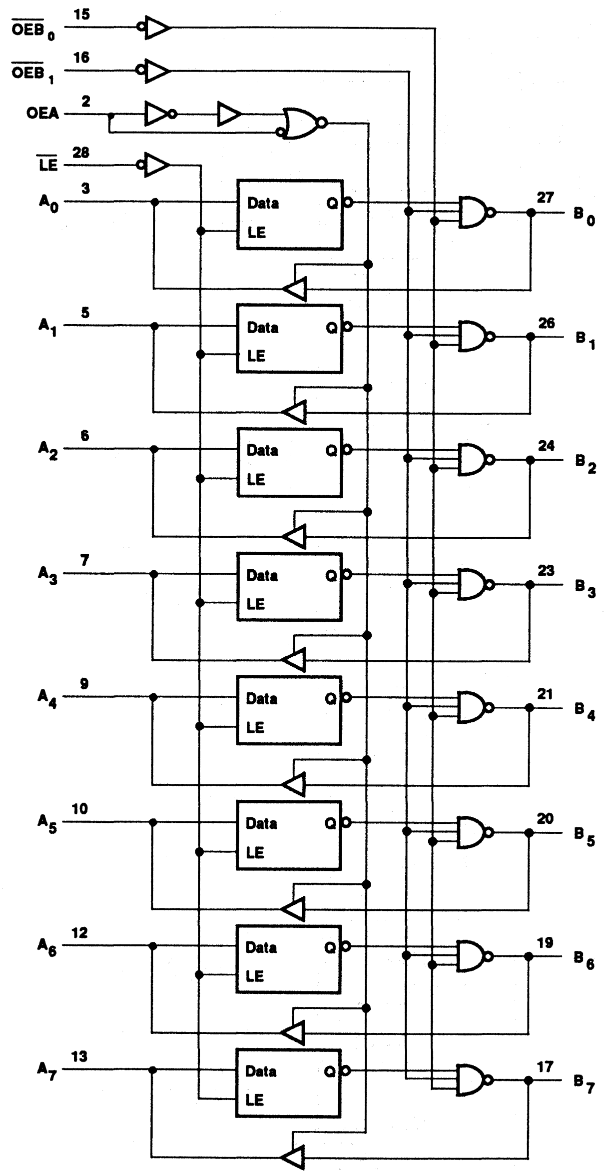
SYMBOL	PINS	TYPE	NAME AND FUNCTION
$A_0 - A_7$	3, 5, 6, 7, 9, 10, 12, 13	I/O	PNP latched input / 3-state output (with V_X control option)
$B_0 - B_7$	27, 26, 24, 23, 21, 20, 19, 17	I/O	Data input with special threshold circuitry to reject noise / Open Collector output, High current drive
$\overline{OEB}_0$	15	Input	Enables the B outputs when both pins are Low
$\overline{OEB}_1$	16	Input	
OEA	2	Input	Enables the A outputs when High
$\overline{LE}$	28	Input	Latched when High (a special delay feature is built in for proper enabling times)
V_X	14	Input	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{CC}$ for normal use)

LOGIC DIAGRAM 74F8960



V_{CC} = Pin 1 V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

LOGIC DIAGRAM 74F8961



V_{CC} = Pin 1 V_X = Pir
GND = Pin 4, 8, 11, 18, 22, 25

FUNCTION TABLE 74F8960

INPUTS						LATCH	OUTPUTS		MODE
A_n	B_n*	$\overline{LE}$	OEA	$\overline{OEB_0}$	$\overline{OEB_1}$	STATE	A_n	B_n	
H	X	L	L	L	L	H	Z	L	A 3-state, Data from A to B
L	X	L	L	L	L	L	Z	H**	
X	X	H	L	L	L	Q_n	Z	$\overline{Q}_n$	A 3-state, Latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	L[2]	L	Z[2]	Preconditioned Latch enabling data transfer from B to A
–	L	H	H	L	L	L[2]	H	Z[2]	
–	–	H	H	L	L	Q_n	$\overline{Q}_n$	$\overline{Q}_n$	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3-state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Q_n	Z	Z	
–	H	L	H	H	X	H	L	Z	B 3-state, Data from B to A
–	L	L	H	H	X	L	H	Z	
–	H	H	H	H	X	Q_n	L	Z	
–	L	H	H	H	X	Q_n	H	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3-state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Q_n	Z	Z	
–	H	L	H	X	H	H	L	Z	B 3-state, Data from B to A
–	L	L	H	X	H	L	H	Z	
–	H	H	H	X	H	Q_n	L	Z	
–	L	H	H	X	H	Q_n	H	Z	

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High Impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB_0}$ and $\overline{OEB_1}$ are Low and $\overline{LE}$ is High.
H** = Goes to level of pullup voltage.
B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to Low state.

FUNCTION TABLE. 74F8961

INPUTS						LATCH	OUTPUTS		MODE
A_n	B_n*	$\overline{LE}$	OEA	$\overline{OEB_0}$	$\overline{OEB_1}$	STATE	A_n	B_n	
H	X	L	L	L	L	H	Z	H**	A 3-state, Data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Q_n	Z	Q_n	A 3-state, Latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	H (2)	H	Z (2)	Preconditioned Latch enabling data transfer from B to A
–	L	H	H	L	L	H (2)	L	Z (2)	
–	–	H	H	L	L	Q_n	Q_n	Q_n	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3-state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Q_n	Z	Z	
–	H	L	H	H	X	H	H	Z	B 3-state, Data from B to A
–	L	L	H	H	X	L	L	Z	
–	H	H	H	H	X	Q_n	H	Z	
–	L	H	H	H	X	Q_n	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3-state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Q_n	Z	Z	
–	H	L	H	X	H	H	H	Z	B 3-state, Data from B to A
–	L	L	H	X	H	L	L	Z	
–	H	H	H	X	H	Q_n	H	Z	
–	L	H	H	X	H	Q_n	L	Z	

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High Impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB_0}$ and $\overline{OEB_1}$ are Low and $\overline{LE}$ is High.
H** = Goes to level of pullup voltage.
B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_X	Threshold control		-0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB_n}$, OEA, $\overline{LE}$	-0.5 to +7.0	V
		A_0 - A_7, B_0 - B_7	-0.5 to 5.5	
I_{IN}	Input current		-40 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	A_0 - A_7	48	mA
		B_0 - B_7	200	
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except B_0 - B_7	2.0			V
		B_0 - B_7	1.625			
V_{IL}	Low-level input voltage	Except B_0 - B_7			0.8	V
		B_0 - B_7			1.475	
I_{IK}	Input clamp current	Except A_0 - A_7			-18	mA
		A_0 - A_7			-40	
I_{OH}	High-level output current	A_0 - A_7			-3	mA
I_{OL}	Low-level output current	A_0 -A_7			24	mA
		B_0 - B_7			100	
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High level output current	$B_0 - B_7$	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	μA
I_{OFF}	Power-off output current	$B_0 - B_7$	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	μA
V_{OH}	High-level output voltage	$A_0 - A_7$[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA, $V_X = V_{CC}$	2.5		V_{CC}	V
				I_{OH} = -0.4mA, V_X = 3.13V & 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	$A_0 - A_7$[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA, $V_X = V_{CC}$			0.5	V
		$B_0 - B_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA			1.15	V
				I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	$A_0 - A_7$	V_{CC} = MIN, $I_I = I_{IK}$				-0.5	V
		Except $A_0 - A_7$	V_{CC} = MIN, $I_I = I_{IK}$				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = 0.0V, V_I = 7.0V				100	μA
		$A_0 - A_7$, $B_0 - B_7$	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 2.7V, $B_n - A_n$ = 0V				20	μA
		$B_0 - B_7$	V_{CC} = MAX, V_I = 2.1V				100	μA
I_{IL}	Low-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 0.5V				-20	μA
		$B_0 - B_7$	V_{CC} = MAX, V_I = 0.3V				-100	μA
$I_{OZH} + I_{IH}$	Off-state output current, High-level voltage applied	$A_0 - A_7$	V_{CC} = MAX, V_O = 2.7V				70	μA
$I_{OZL} + I_{IL}$	Off-state output current, Low-level voltage applied	$A_0 - A_7$	V_{CC} = MAX, V_O = 0.5V				-70	μA
I_X	High-level control current		V_{CC} = MAX, $V_X = V_{CC}$, $\overline{LE}$ = OEA = $\overline{OEB}_n$ = 2.7V, $A_0 - A_7$ = 2.7V, $B_0 - B_7$ = 2.0V		-100		100	μA
			V_{CC} = MAX, V_X = 3.13V & 3.47 V, $\overline{LE}$ = OEA = 2.7V, $\overline{OEB}_n$ = $A_0 - A_7$ = 2.7V, $B_0 - B_7$ = 2.0V		-10		10	mA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$ only	V_{CC} = MAX, B_n = 1.6V, OEA = 2.0V, $\overline{OEB}_n$ = 2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			70	100	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			100	145	mA
		I_{CCZ}	V_{CC} = MAX, V_{IL} = 0.5V			80	100	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, $V_X = V_{CC}$ for all test conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH}=1.6V and V_{IL}=1.3V.

AC ELECTRICAL CHARACTERISTICS for 74F8960

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1, 2	5.5 6.0	7.5 7.5	12.0 10.5	5.0 6.0	12.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA to A	Waveform 4.5	8.0 8.5	10.5 12.0	14.5 14.5	7.5 8.5	15.5 17.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA to A	Waveform 4.5	2.0 2.0	4.5 4.5	7.0 7.5	2.0 2.0	7.5 8.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_D = 30pF, R_U = 9Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1, 2	2.0 3.5	4.0 6.0	7.0 8.0	2.0 3.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to B	Waveform 1, 2	3.0 4.0	5.0 6.0	8.5 9.0	2.5 3.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}_n$ to B	Waveform 1, 2	2.5 4.5	4.5 7.5	7.5 10.5	1.5 3.5	8.5 10.5	ns
t_{TLH} t_{THL}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	4.5 4.5	ns

AC SETUP REQUIREMENTS for 74F8960

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time A to $\overline{LE}$	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time A to $\overline{LE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(L)$	$\overline{LE}$ pulse width, Low	Waveform 3	6.0			6.0		ns

Futurebus Transceivers

FAST 74F8960, 74F8961

AC ELECTRICAL CHARACTERISTICS for 74F8961

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1, 2	5.5 6.0	7.5 7.5	12.0 10.5	5.0 6.0	12.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA to A	Waveform 4.5	8.0 8.5	10.5 12.0	14.5 14.5	7.5 8.5	15.5 17.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA to A	Waveform 4.5	2.0 2.0	4.5 4.5	7.0 7.5	2.0 2.0	7.5 8.0	ns

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_D = 30pF$, $R_U = 9\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_D = 30pF$, $R_U = 9\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1, 2	2.0 3.5	4.0 6.0	7.0 8.0	2.0 3.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to B	Waveform 1, 2	3.0 4.0	5.0 6.0	8.5 9.0	2.5 3.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB_n}$ to B	Waveform 1, 2	2.5 4.5	4.5 7.5	7.5 10.5	1.5 3.5	8.5 10.5	ns
t_{TLH} t_{THL}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	4.5 4.5	ns

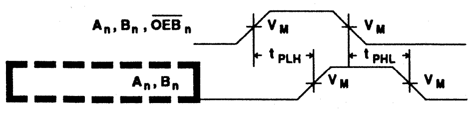
AC SETUP REQUIREMENTS for 74F8961

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time A to $\overline{LE}$	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time A to $\overline{LE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(L)$	$\overline{LE}$ pulse width, Low	Waveform 3	6.0			6.0		ns

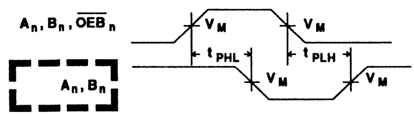
Futurebus Transceivers

FAST 74F8960, 74F8961

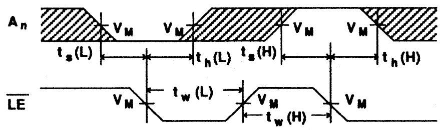
AC WAVEFORMS



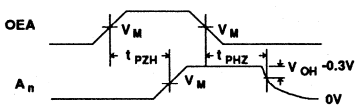
Waveform 1. Propagation Delay For Data To Output



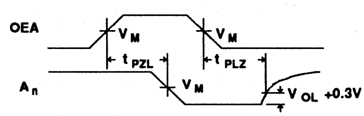
Waveform 2. Propagation Delay For Data To Output



Waveform 3. Data Setup And Hold Times And $\overline{LE}$ Pulse Widths



Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

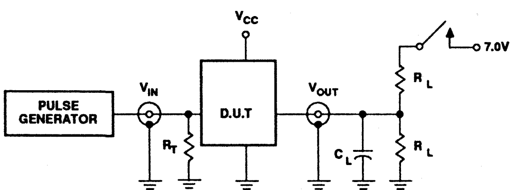


Waveform 5 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

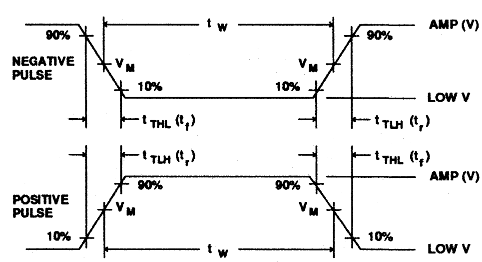
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs On A Port

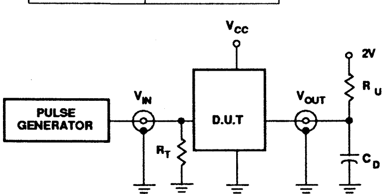


$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit For Outputs On B Port

FAMILY 74F	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_U = Pull up resistor; see AC CHARACTERISTICS for value.

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ECN No.	99390
Date of issue	April 18, 1990
Status	Product Specification
FAST Products	

FAST 74F8962, 74F8963

Futurebus Transceivers

74F8962 9-Bit Latched Bidirectional Futurebus Transceiver, INV (OC)
74F8963 9-Bit Latched Bidirectional Futurebus Transceiver, NINV (OC)

TYPE	TYPICAL PROPAGATION DELAY	MAX SUPPLY CURRENT (TOTAL)
74F8962	6.5ns	90mA
74F8963	5.5ns	90mA

FEATURES

- **Octal Latched Transceiver**
- **Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms**
- **High drive (100mA) open collector drivers on B-port**
- **Reduced voltage swing (1 volt) produces less noise and reduces power consumption**
- **High speed operation enhances performance of backplane buses and facilitates incident wave switching**
- **Compatible with IEEE 896 Futurebus Standard**
- **Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity**
- **Multiple GND pins minimize ground bounce**
- **Glitch-free power up / power down operation**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
44-Pin Quad Flatpack[1]	N74F8962Y, N74F8963Y
44-Pin PLCC	N74F8962A, N74F8963A

NOTE 1: Flatpack package is not available at this time.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
AI_0 - AI_8	PNP latched inputs	1.0/0.033	20µA/20µA
B_0 - B_8	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable inputs (active Low)	1.0/0.033	20µA/20µA
$\overline{LEAB}$, $\overline{LEBA}$	Latch Enable inputs (active Low)	1.0//0.033	20µA/20µA
AO_0 - AO_8	3-State outputs	150/40	3mA/24mA
B_0 - B_8	Open Collector outputs	OC*/166.7	OC*/100mA

NOTES:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
* OC = Open Collector

DESCRIPTION

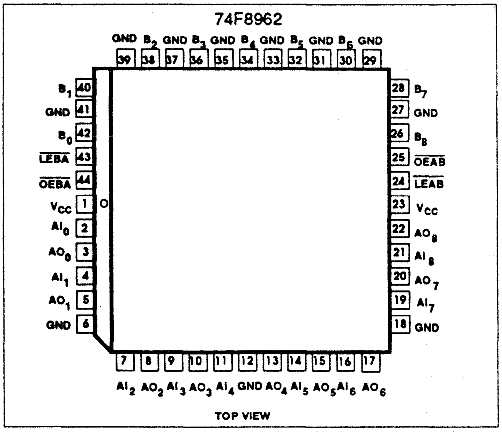
The 74F8962 and 74F8963 are octal bidirectional latched transceivers and are intended to provide the electrical interface to a high performance wired-OR bus. The B port inverting drivers are low-capacitance open collector with controlled ramp and are designed to sink 100 mA from 2 volts. The B port receivers have a 150 mV threshold region.

The B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading.

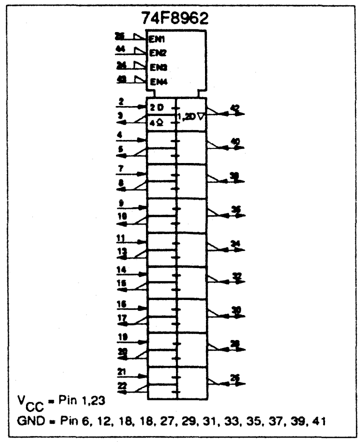
Incident wave switching TO 9 ohm is guaranteed. The voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.
BTL offers low power consumption, low ground bounce, low EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.
The 74F8962 and 74F8963 A ports have TTL 3-State drivers and TTL receivers with a latch function.

74F8963 is the non-inverting version of 74F8962.

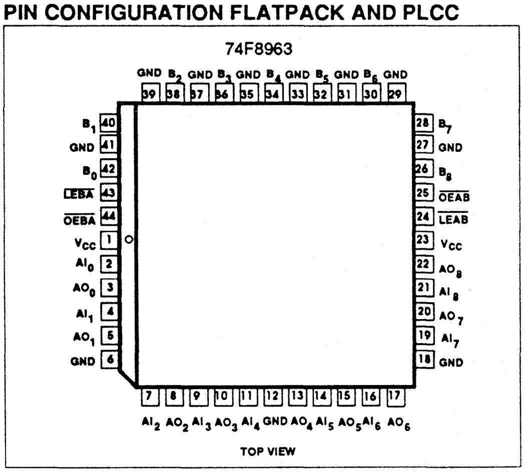
PIN CONFIGURATION FLATPACK and PLCC



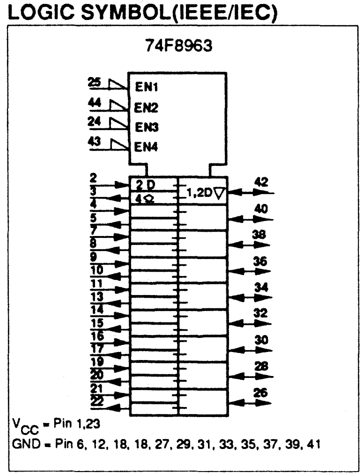
LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION FLATPACK AND PLCC



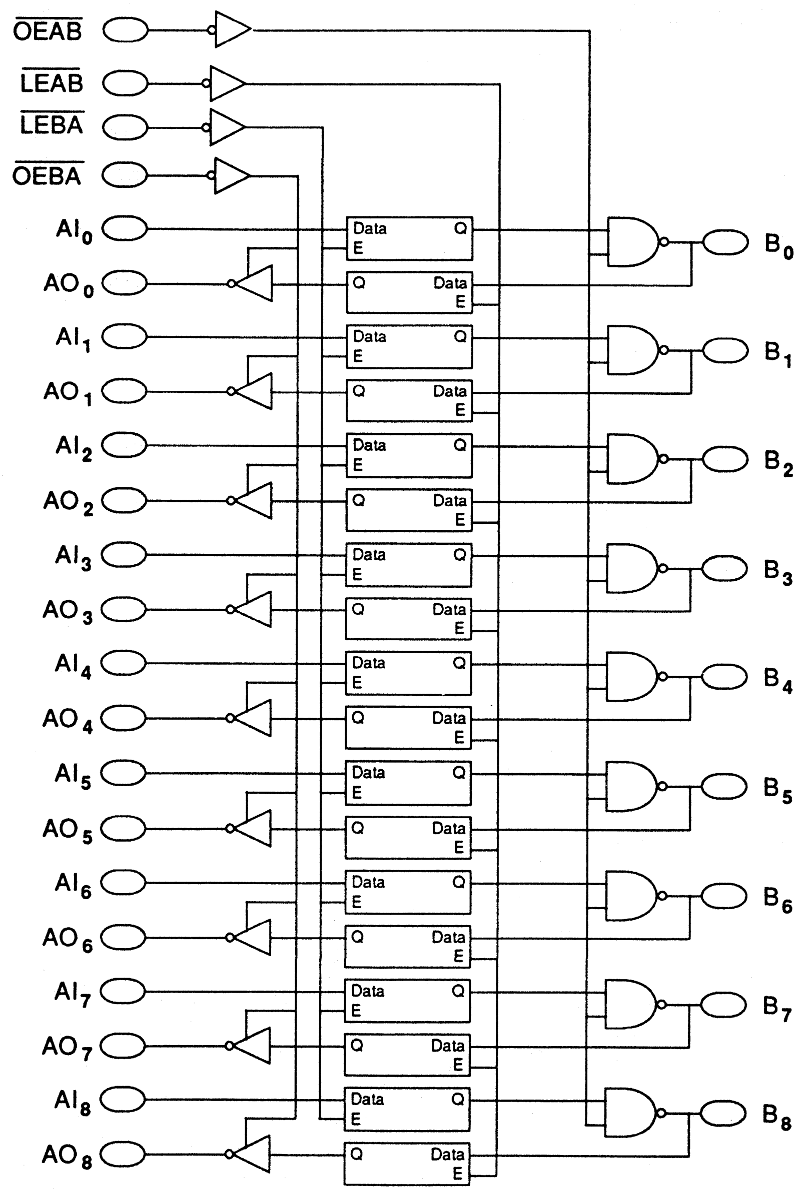
LOGIC SYMBOL(IEEE/IEC)



PIN DESCRIPTION

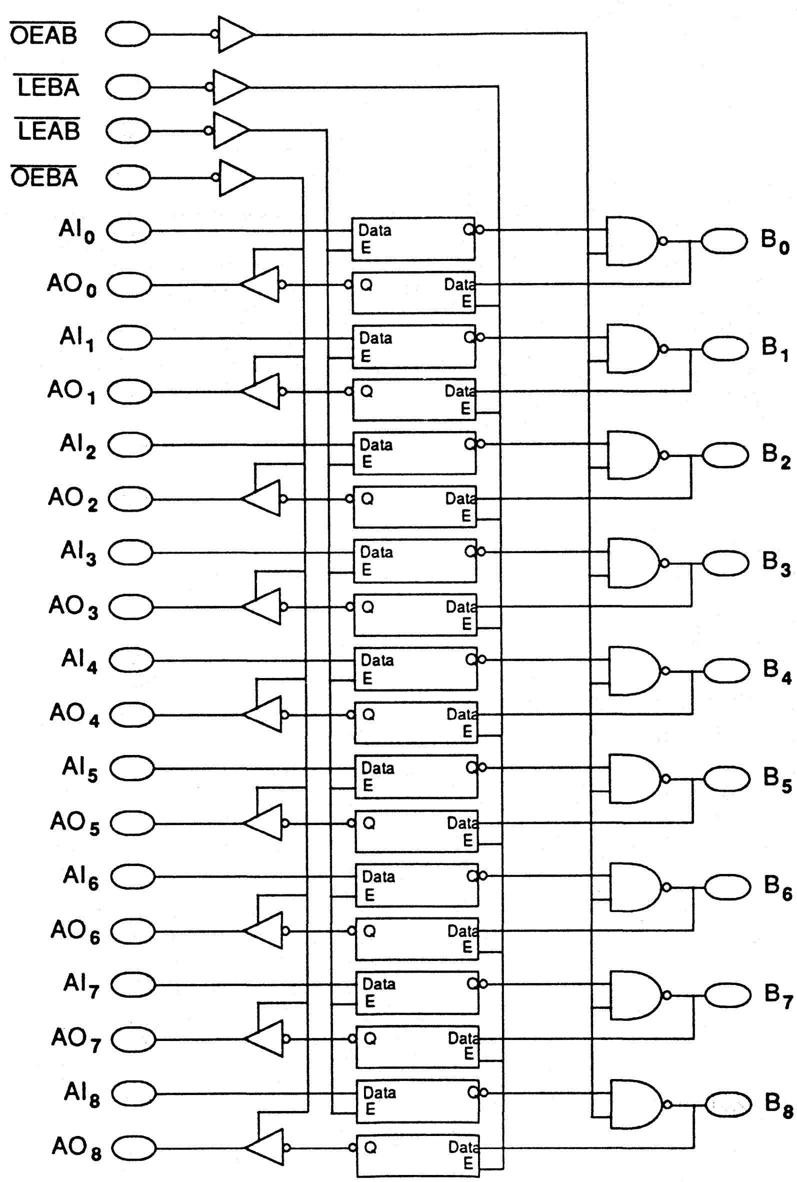
SYMBOL	PINS	TYPE	NAME AND FUNCTION
AI_0 - AI_8	2, 4, 7, 9, 11,14, 16, 19, 21	Input	PNP latched inputs
B_0 - B_8	42, 40, 38, 36, 34, 32, 30, 28, 26	I/O	Data input / Open Collector outputs. High current drives.
$\overline{OEAB}$	25	Input	Output Enable input. Enables the B outputs when Low.
$\overline{OEBA}$	44	Input	Output Enable input. Enables the A outputs when Low.
$\overline{LEAB}$	24	Input	Latch Enable input. Enables the AB latches Low.
$\overline{LEBA}$	43	Input	Latch Enable input. Enables the BA latvches Low
AO_0 - AO_8	3, 5, 8, 10, 13, 15, 17, 20, 22	Output	TTL 3-state outputs
GND	6, 12, 18, 27, 29, 31, 33, 35, 37, 39,41	Ground	Grounds
V_{CC}	1, 23	Power	Positive supply voltages

LOGIC DIAGRAM 74F8962



V_{CC} = Pin 1,23
GND = Pin 6, 12, 18, 27, 29, 31, 33, 35, 37, 39, 41

LOGIC DIAGRAM 74F8963



V_{CC} = Pin 1,23
GND = Pin 6, 12, 18, 27, 29, 31, 33, 35, 37, 39, 41

FUNCTION TABLE 74F8962

INPUTS						LATCH STATES		OUTPUTS		MODE
AI	B_n*	$\overline{LEAB}$	$\overline{LEBA}$	$\overline{OEAB}$	$\overline{OEBA}$	AB	BA	AO_n	B_n	
H	H	L	L	H	H	H	H	Z	X	B and AO disabled
L	L	L	L	H	H	L	L	Z	X	
X	X	H	H	H	H	Q_n	Q_n	Z	X	
H	–	L	X	L	H	H	Q_n	Z	L	AO 3-state, transparent data from AI to B
L	-	L	X	L	H	L	Q_n	Z	H**	
X	H	X	L	H	L	Q_n	H	L	X	B disabled, transparent data from B to AO
X	L	X	L	H	L	Q_n	L	H	X	
X	X	H	X	L	H	Q_n	Q_n	Z	$\overline{Q}_n$	AO 3-state, latched data to B
X	X	X	H	H	L	Q_n	Q_n	$\overline{Q}_n$	X	B disabled, latched data to AO
X	X	H	H	L	L	Q_n	Q_n	$\overline{Q}_n$	$\overline{Q}_n$	Latched state to AO and B
H	-	L	L	L	L	H	L	H	L	Read back from AI to B to AO (both latches transparent)
L	-	L	L	L	L	L	H	L	H**	

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High Impedance (OFF) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LEXX}$ transition
H** = Goes to level of pullup voltage.
B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to Low state.

FUNCTION TABLE 74F8963

INPUTS						LATCH STATES		OUTPUTS		MODE
AI	B_n*	$\overline{LEAB}$	$\overline{LEBA}$	$\overline{OEAB}$	$\overline{OEBA}$	AB	BA	AO_n	B_n	
H	H	L	L	H	H	L	L	Z	X	B and AO disabled
L	L	L	L	H	H	H	H	Z	X	
X	X	H	H	H	H	$\overline{Q}_n$	$\overline{Q}_n$	Z	X	
H	–	L	X	L	H	L	$\overline{Q}_n$	Z	H	AO 3-state, transparent data from AI to B
L	-	L	X	L	H	H	$\overline{Q}_n$	Z	L	
X	H	X	L	H	L	$\overline{Q}_n$	L	H	X	B disabled, transparent data from B to AO
X	L	X	L	H	L	$\overline{Q}_n$	H	L	X	
X	X	H	X	L	H	$\overline{Q}_n$	$\overline{Q}_n$	Z	$\overline{Q}_n$	AO 3-state, latched data to B
X	X	X	H	H	L	$\overline{Q}_n$	$\overline{Q}_n$	Q_n	X	B disabled, latched data to AO
X	X	H	H	L	L	$\overline{Q}_n$	$\overline{Q}_n$	Q_n	Q_n	Latched state to AO and B
H	-	L	L	L	L	L	L	H	H**	Read back from AI to B to AO (both latches transparent)
L	-	L	L	L	L	H	H	L	L	

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High Impedance (OFF) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LEXX}$ transition
H** = Goes to level of pullup voltage.
B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEBA}$, $\overline{OEAB}$, $\overline{LEBA}$, $\overline{LEAB}$	-0.5 to +7.0	V
		A_0 - A_8, B_0 - B_8	-0.5 to +5.5	
I_{IN}	Input current		-40 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	AO_0 - AO_8	48	mA
		B_0 - B_8	200	
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except B_0 - B_8	2.0			V
		B_0 - B_8	1.62			
V_{IL}	Low-level input voltage	Except B_0 - B_8			0.8	V
		B_0 - B_8			1.47	
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	AO_0 - AO_8			-3	mA
I_{OL}	Low-level output current	AO_0 - AO_8			24	mA
		B_0 - B_8			100	
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS Min	Typ[2]	Max	UNIT
I_{OH}	High level output current	$B_0 - B_8$	V_{CC} = MAX, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V			100	µA
I_{OFF}	Power-off output current	$B_0 - B_8$	V_{CC} = 0.0V, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V			100	µA
V_{OH}	High-level output voltage	$AO_0 - AO_8$[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -3mA	2.5		V_{CC}	V
V_{OL}	Low-level output voltage	$AO_0 - AO_8$[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 24mA			0.5	V
		$B_0 - B_8$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 100mA	0.75	1.0	1.10	V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 4mA	0.4			V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEAB}$, $\overline{LEAB}$, $\overline{LEBA}$, $AI_0 - AI_8$	V_{CC} = MAX, V_I = 7.0V			100	µA
		$B_0 - B_8$	V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IH}	High-level input current	$\overline{OEAB}$, $\overline{OEAB}$, $\overline{LEAB}$, $\overline{LEBA}$, $AI_0 - AI_8$	V_{CC} = MAX, V_I = 2.7V			20	µA
		$B_0 - B_8$	V_{CC} = MAX, V_I = 2.1V			100	µA
I_{IL}	Low-level input current	$\overline{OEAB}$, $\overline{OEAB}$, $\overline{LEAB}$, $\overline{LEBA}$, $AI_0 - AI_8$	V_{CC} = MAX, V_I = 0.5V			-20	µA
		$B_0 - B_8$	V_{CC} = MAX, V_I = 0.3V			-100	µA
I_{OZH}	Off-state output current, High-level voltage applied	$AO_0 - AO_8$	V_{CC} = MAX, V_O =2.7V			50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	$AO_0 - AO_8$	V_{CC} = MAX, V_O =0.5V			-50	µA
I_{OS}	Short-circuit output current[3] 'F8962	$AO_0 - AO_8$ only	V_{CC} = MAX, B_n = 1.3V, $\overline{OEBA}$ = 0.8V, $\overline{OEB_n}$ = 2.7V	-60		-150	mA
	Short-circuit output current[3] 'F8963		V_{CC} = MAX, B_n = 1.8V, $\overline{OEBA}$ = 0.8V, $\overline{OEB_n}$ = 2.7V				
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		80	110	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V		105	145	mA
		I_{CCZ}			80	110	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH}=1.8V and V_{IL}=1.3V.

AC ELECTRICAL CHARACTERISTICS FOR 74F8962

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS							UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_A =0°C to +70°C V_{CC} = 5V ±5% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B_n to AO_n	Waveform 1, 2	5.0 3.5	7.0 5.5	10.0 8.5	4.5 3.5	11.0 8.5	4.5 3.5	10.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to AO_n	Waveform 1,2	5.5 4.5	7.0 6.5	10.0 9.5	5.0 4.5	10.0 9.5	5.0 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low $\overline{OEBA}$ to AO_n	Waveform 5,6	7.5 8.5	9.5 10.5	12.5 13.0	6.5 7.5	13.5 14.5	6.5 7.5	13.0 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low $\overline{OEBA}$ to AO_n	Waveform 5,6	3.5 4.5	5.5 6.5	8.5 9.5	2.5 4.0	10.0 10.0	2.5 4.0	9.0 9.5	ns
t_{RSKEW}	Skew between receivers in same package	Waveform 4		1.5	2.5		4.0		4.0	ns

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS							UNIT
			T_A = +25°C V_{CC} = 5V C_D= 30pF R_U = 9Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_D = 30pF R_U = 9Ω		T_A =0°C to +70°C V_{CC} = 5V ±5% C_D = 30pF R_U = 9Ω		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay AI_n to B_n	Waveform 1, 2	3.5 4.0	5.5 6.0	8.5 9.5	3.0 3.5	9.0 10.5	3.0 3.5	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to B_n	Waveform 1, 2	4.0 5.0	6.0 7.0	8.5 10.5	3.5 5.0	9.5 10.5	3.5 5.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Output Enable/Disable time $\overline{OEAB}$ to B_n	Waveform 1	3.5 3.0	5.0 4.0	8.0 8.0	3.0 2.5	8.5 8.5	3.0 2.5	8.0 8.5	ns
t_{TLH} t_{THL}	Transition time, B_n port 10% to 90%, 90% to 10%	Test Circuit and Waveforms	1.0 1.0	1.2 2.0	1.6 2.5	1.0 1.0	2.5 3.5	1.0 1.0	2.5 3.5	ns
t_{DSKEW}	Skew between drivers in same package	Waveform 4		0.5	2.0		3.0		3.0	ns

AC SETUP REQUIREMENTS FOR 74F8962

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_A =0°C to +70°C V_{CC} = 5V ±5% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time AI_n to $\overline{LEAB}$	Waveform 3	3.0 1.0			3.5 2.0		3.0 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time AI_n to $\overline{LEAB}$	Waveform 3	3.0 0.0			3.5 0.0		3.0 0.0		ns
$t_s(H)$ $t_s(L)$	Set-up time B_n to $\overline{LEBA}$	Waveform 3	2.0 1.0			2.5 1.0		2.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time B_n to $\overline{LEBA}$	Waveform 3	3.0 1.5			3.5 2.0		3.0 2.0		ns
$t_w(L)$	$\overline{LEAB}$ or $\overline{LEBA}$ Pulse width, Low	Waveform 3	4.5			4.5		4.5		ns

AC ELECTRICAL CHARACTERISTICS FOR 74F8963

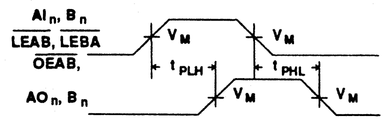
SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS							UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_A =0°C to +70°C V_{CC} = 5V ±5% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B_n to AO_n	Waveform 1, 2	3.5 2.5	5.5 4.0	8.0 7.0	3.0 2.0	9.0 7.5	3.0 2.0	8.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to AO_n	Waveform 1,2	6.0 4.0	7.5 5.5	10.0 8.5	5.0 3.5	11.5 9.0	5.0 3.5	10.0 8.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low $\overline{OEBA}$ to AO_n	Waveform 5,6	9.0 10.0	11.0 12.0	14.0 15.0	8.5 9.0	15.5 17.0	8.5 9.0	14.5 15.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low $\overline{OEBA}$ to AO_n	Waveform 5,6	4.0 5.5	6.0 7.0	9.0 10.0	3.0 5.0	10.5 11.0	3.0 5.0	9.5 10.0	ns
t_{RSKEW}	Skew between receivers in same package	Waveform 4		1.5	2.0		4.0		4.0	ns

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS							UNIT
			T_A = +25°C V_{CC} = 5V C_D = 30pF R_U = 9Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_D = 30pF R_U = 9Ω		T_A =0°C to +70°C V_{CC} = 5V ±5% C_D = 30pF R_U = 9Ω		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay AI_n to B_n	Waveform 1, 2	2.0 2.0	4.0 3.5	6.5 6.5	1.5 1.5	7.0 6.5	2.0 2.0	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to B_n	Waveform 1, 2	3.5 2.5	5.0 4.0	8.0 7.0	3.0 2.0	8.5 8.0	3.5 2.5	8.5 8.0	ns
t_{PLH} t_{PHL}	Output Enable/Disable time $\overline{OEAB}$ to B_n	Waveform 1	3.5 3.0	5.5 5.0	8.0 7.5	2.5 2.5	8.5 8.5	2.5 2.5	8.0 8.0	ns
t_{TLH} t_{THL}	Transition time, B_n port 10% to 90%, 90% to 10%	Test Circuit and Waveforms	1.0 1,0	1.2 2.0	1.6 2.5	1.0 1.0	2.5 3.5	1.0 1.0	2.5 3.5	ns
t_{DSKEW}	Skew between drivers in same package	Waveform 4		0.5	2.0		3.0		3.0	ns

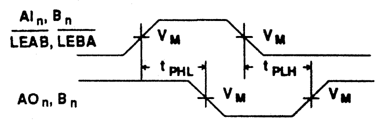
AC SETUP REQUIREMENTS FPR 74F8963

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_A =0°C to +70°C V_{CC} = 5V ±5% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time AI_n to $\overline{LEAB}$	Waveform 3	4.0 1.0			4.5 1.5		4.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time AI_n to $\overline{LEAB}$	Waveform 3	2.5 0.0			3.0 0.0		2.5 0.0		ns
$t_s(H)$ $t_s(L)$	Set-up time B_n to $\overline{LEBA}$	Waveform 3	2.0 0.0			2.5 1.0		2.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time B_n to $\overline{LEBA}$	Waveform 3	2.5 1.0			3.0 1.5		3.0 1.0		ns
$t_w(L)$	$\overline{LEAB}$ or $\overline{LEBA}$ Pulse width, Low	Waveform 3	4.5			5.5		5.5		ns

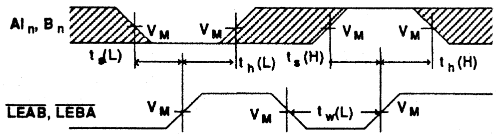
AC WAVEFORMS



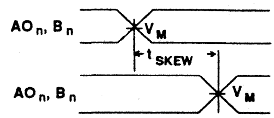
Waveform 1. Propagation Delay For Data Or Output Enable Or Latch Enable To Output



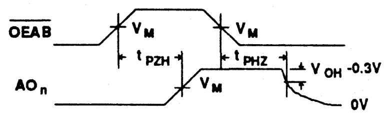
Waveform 2. Propagation Delay For Data Or Latch Enable To Output



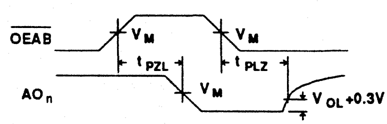
Waveform 3. Data Setup And Hold Times And LEAB/LEBA Pulse Widths



Waveform 4. Propagation delay skew and output to output skew



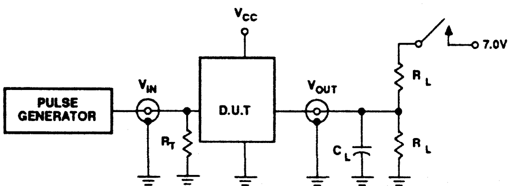
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



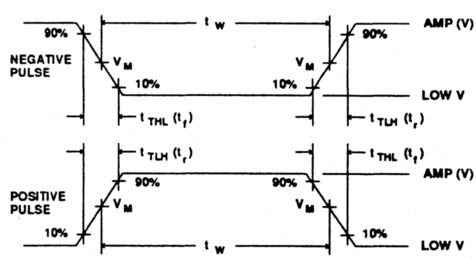
Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs On A Port

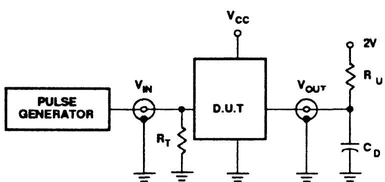


$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit For Outputs On B Port

FAMILY 74F	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_U = Pull up resistor; see AC CHARACTERISTICS for value.

Document No.	853-1157
ECN No.	97652
Date of issue	September 15, 1989
Status	Product Specification
FAST Products	

FAST 74F30240,74F30244
30Ω Line Drivers

'F30240 Octal 30Ω Line Driver With Enable, Inverting (Open Collector)
'F30244 Octal 30Ω Line Driver With Enable, Non-Inverting (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30240	9.5ns	62.5mA
74F30244	10.5ns	69mA

FEATURES

- **Ideal for driving transmission lines or backplanes. 160mA I_{OL} ideal for applications with impedance as low as 30Ω**
- **Guaranteed threshold voltages on the incident wave while driving line as low as 30Ω.**
- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Ideal for applications which require high output drive and minimal bus loading**
- **Octal interface**
- **'F30240 Inverting**
- **'F30244 Non-Inverting**
- **Open-Collector outputs sink 160mA**
- **Multiple side pins are used for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)**
- **Available in 24-pin standard slim DIP (300mil) plastic, SOL or CERDIP packages**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Cerdip (300 mil)	N74F30240F, N74F30244F
24-Pin Plastic Slim DIP(300 mil)[1]	N74F30240N, N74F30244N
24-Pin Plastic SOL[2]	N74F30240D, N74F30244D

NOTE:
1.Thermal mounting techniques are recommended.

2. Because of the high current sinking capability of these parts, the SOL package should only be used under the following conditions: a) 50% duty cycle AND b) 3/5 of remaining 50% driving ≤ 100 mA (leaving the remaining 2/5 of the to drive ≤ 160 mA) OR c) use ≥ 450 linear feet per minute forced air or other thermal mounting techniques.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_7	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$- $\overline{OE}_1$	Output Enable inputs (active Low)	1.0/0.033	20μA/20μA
$\overline{Q}_0$- $\overline{Q}_7$	Data outputs (OC) for 'F30240	OC/266.7	OC/160mA
Q_0- Q_7	Data outputs (OC) for 'F30244	OC/266.7	OC/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC = Open Collector

DESCRIPTION

The 74F30240/F30244 are high current open collectors octal buffers composed of eight inverters. The 'F30240 has inverting data paths and the 'F30244 has non-inverting paths. Each device has eight inverters with two Output Enables($\overline{OE}_0$, $\overline{OE}_1$) each controlling four outputs. Both drivers are designed to deal with the low-impedance transmission line effects found on printed circuit boards when fast edge rates are used. The 160 mA I_{OL} provides ample power to achieve TTL switching voltages on the incident wave.

Document No.	853-1200
ECN No.	99391
Date of issue	April 18, 1990
Status	Product Specification
FAST Products	

FAST 74F30245,74F30640

Transceivers

74F30245 Octal 30Ω Transceiver Non-Inverting
(Open Collector With Enable + 3-State)
74F30640 Octal 30Ω Transceiver Inverting
(Open Collector With Enable + 3-State)

FEATURES

- **High impedance NPN base inputs for reduced loading**
- **Ideal for applications which require high output drive and minimal bus loading**
- **Octal bidirectional bus interface**
- **'F30245 Non-Inverting**
- **'F30640 Inverting**
- **Choice of outputs:**
  Open collectors (B_0-B_7) and 3-states(A_0-A_7)
- **Open-Collector outputs sink 160mA**
- **160mA I_{OL} ideal for low-impedance applications and transmission line effects with impedance as low as 30Ω**
- **3-state buffer outputs sink 24mA**
- **Multiple side pins are used for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)**
- **Available in 24-pin standard slim DIP (300mil) plastic or CERDIP packages**
- **Flow through pinout structure facilitates PC board layout**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30245	5.5ns	90mA
74F30640	5.0ns	85mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Cerdip (300 mil)	N74F30245F, N74F30640F
24-Pin Plastic Slim DIP[1]	N74F30245N, N74F30640N

NOTE:
1.Thermal mounting techniques are recommended.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7	Data inputs	3.5/0.1167	70µA/70µA
B_0- B_7	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable input (active Low)	2.0/0.0667	40µA/40µA
$\overline{T}$/R	Transmit/Receive input	2.0/0.0667	40µA/40µA
A_0- A_7	Data outputs (3-state)	150/40	3.0mA/24mA
B_0- B_7	Data outputs (OC)	OC/266.7	OC/160mA

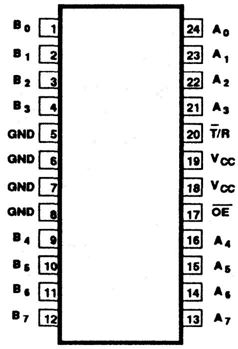
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC = Open Collector

DESCRIPTION

The 74F30245/F30640 are high current octal transceivers. The 'F30245 has non-inverting data paths and the 'F30640 has inverting paths. The B outputs are open collector with 160mA I_{OL} while the A outputs are 3-state with 24mA I_{OL}.Both transceivers are designed to deal with the low-impedance transmission line effects found on printed circuit boards when fast edge rates are used. The 160 mA I_{OL} provides ample power to achieve TTL switching voltages on the incident wave. if the power is removed from the device.

PIN CONFIGURATION

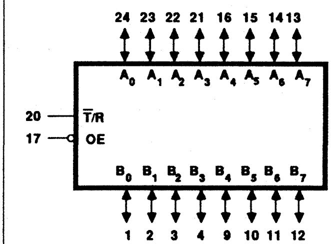
'F30245



TOP VIEW

LOGIC SYMBOL

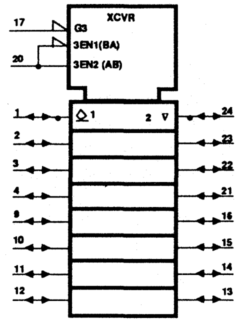
'F30245



V_{CC} = Pin 18,19
GND = Pin 5,6,7,8

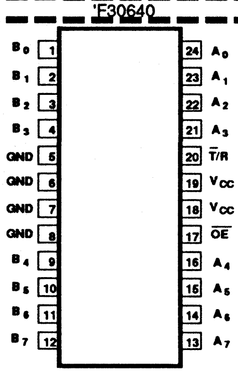
LOGIC SYMBOL(IEEE/IEC)

'F30245



PIN CONFIGURATION

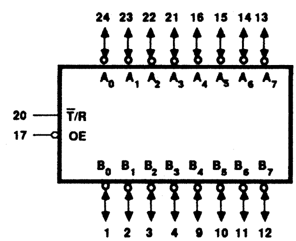
'F30640



TOP VIEW

LOGIC SYMBOL

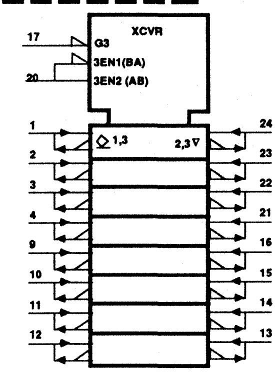
'F30640



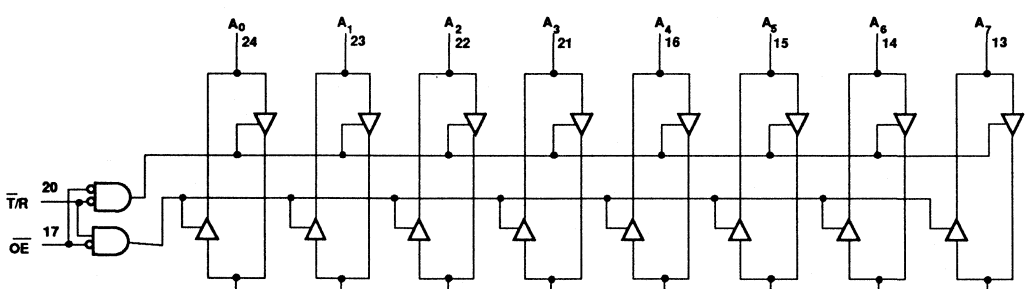
V_{CC} = Pin 18,19
GND = Pin 5,6,7,8

LOGIC SYMBOL(IEEE/IEC)

'F30640



LOGIC DIAGRAM 'F30245



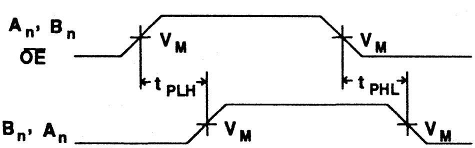
V_{CC}=pin 18, 19
GND=pin 5, 6, 7, 8

AC ELECTRICAL CHARACTERISTICS

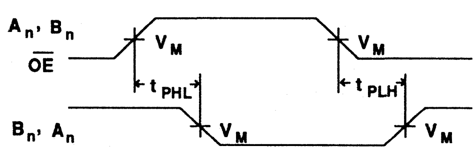
SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
				Min	Typ	Max	Min	Max	
t_{PLH}* t_{PHL}	Propagation delay A_n to B_n	'F30245	Waveform 1,2	7.5 3.0	10.0 4.5	13.0 7.5	7.0 2.5	13.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	'F30245	Waveform 1,2	2.0 2.0	3.5 3.5	6.5 6.0	1.5 1.5	7.0 6.5	ns
t_{PLH}* t_{PHL}	Propagation delay A_n to B_n	'F30640	Waveform 1,2	6.0 1.0	8.0 2.0	12.0 5.0	6.0 1.0	12.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	'F30640	Waveform 1,2	1.0 1.0	2.5 2.0	5.5 5.0	1.0 1.0	6.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ or $\overline{T}$/R to B_n	B_n outputs	Waveform 1,2	6.5 3.5	8.0 5.5	12.0 8.5	6.5 3.0	12.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ or $\overline{T}$/R to A_n	A_n outputs	Waveform 3 Waveform 4	2.5 1.5	4.5 4.0	7.5 8.0	2.0 1.5	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ or $\overline{T}$/R to A_n	A_n outputs	Waveform 3 Waveform 4	1.5 1.0	3.5 3.5	6.5 6.5	1.0 1.0	7.5 7.0	ns

NOTES:
1. See Figure A for Open Collector information.
2. $\overline{T}$/R propagation delays are guaranteed without testing.

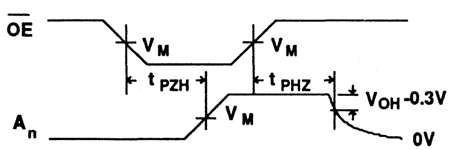
AC WAVEFORMS



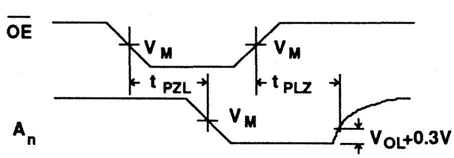
Waveform 1. Propagation Delay For Non-Inverting Output



Waveform 2. Propagation Delay For Inverting Output



Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

Document No.	853-1388
ECN No.	98499
Date of issue	January 8, 1990
Status	Product
FAST Products	

FAST 74F50109

Flip-Flop/Clock Driver

Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop With Metastable Immune Characteristics

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F50109	150 MHz	22mA

FEATURES

- **Metastable Immune Characteristics**
- **Propagation delay skew and output to output skew guaranteed less than 1.5ns**
- **High source current (I_{OH} = 15mA) ideal for clock driver applications**
- **Pinout compatible with 74F109**
- **See 74F5074 for Synchronizing Dual D-Type Flip-Flop**
- **See 74F50728 for Synchronizing Cascaded D-Type Flip-Flop**
- **See 74F50729 for Synchronizing Dual D-Type Flip-Flop with Edge-Triggered Set and Reset**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F50109N
16-Pin Plastic SO	N74F50109D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/0.417	20µA/250µA
$\overline{K}_0$, $\overline{K}_1$	K inputs	1.0/0.417	20µA/250µA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.033	20µA/20µA
$\overline{S}_{D0}$, $\overline{S}_{DI}$	Set inputs (active Low)	1.0/0.033	20µA/20µA
$\overline{R}_{D0}$, $\overline{R}_{DI}$	Reset inputs (active Low)	1.0/0.033	20µA/20µA
Q_0, Q_I, $\overline{Q}_0$, $\overline{Q}_I$	Data outputs	750/33	15mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F50109 is a dual positive edge-triggered JK-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs; also true and complementary outputs.

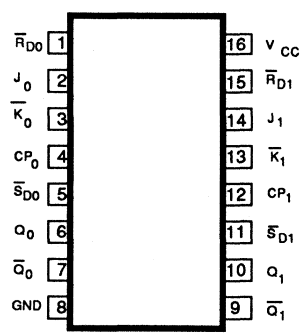
Set ($\overline{S}_{Dn}$) and Reset ($\overline{R}_{Dn}$) are asynchronous active-Low inputs and operate independently of the Clock (CP_n) inputs.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Function Table.

The J and $\overline{K}$ inputs must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays. The J$\overline{K}$ design allows operation as a D flip-flop by tying J and $\overline{K}$ inputs together.

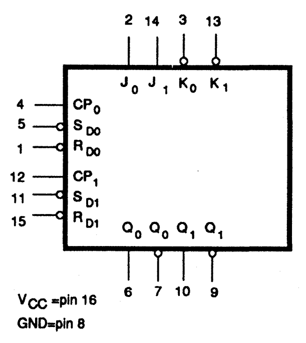
The 74F50109 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability

PIN CONFIGURATION

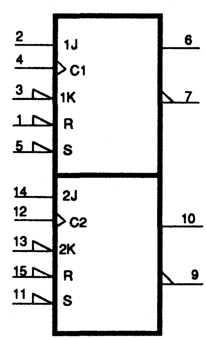


TOP VIEW

LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Flip-Flop/Clock Driver 74F50109

parameters for the 74F50109 are: $t \cong 135$ps and $T_0 \cong 9.8 \times 10^6$sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state .

Metastable Immune Characteristics

Signetics uses the term 'metastable immune' to describe characteristics of some of the products in its FAST family. Specifically the 74F50XXX family presently consists of 4 products which display metastable immune characteristics. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations. This claim is easily verified on the 74F5074. By running two independent signal generators (see Fig. 1) at nearly the same frequency (in this case 10 MHz clock and 10.02 MHz data) the device-under-test can often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

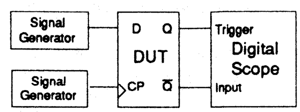
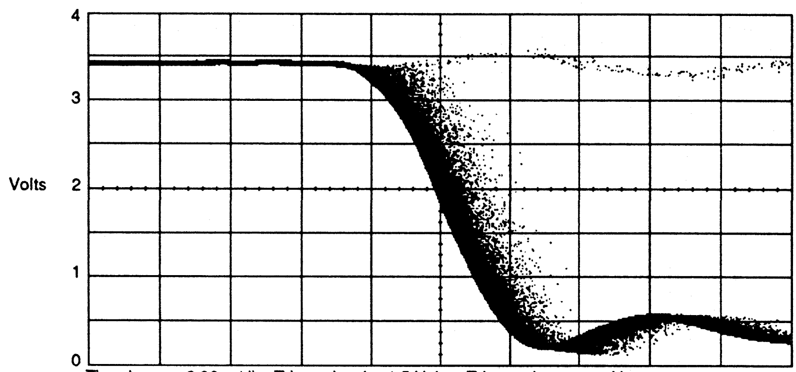


Fig. 1—Test Set up

When the device-under-test is a 74F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Fig. 2.

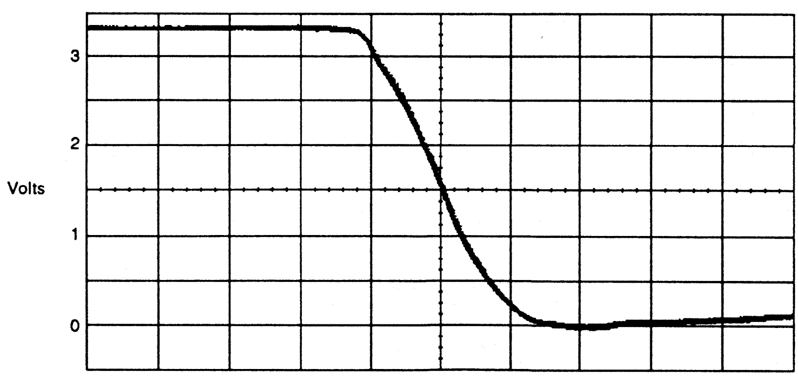
Fig. 2 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5 volt line in the upper right

COMPARISON OF METASTABLE IMMUNE AND NON-IMMUNE CHARACTERISTICS



Time base = 2.00ns/div Trigger level = 1.5 Volts Trigger slope = positive

Fig. 2—74F74 $\overline{Q}$ output triggered by Q output, setup and hold times violated



Time base = 2.00ns/div Trigger level = 1.5 Volts Trigger slope = positive

Fig. 3—74F5074 $\overline{Q}$ output triggered by Q output, setup and hold times violated

hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.
When the device-under-test is a metastable immune part, such as the 74F5074, the waveform will appear as in Fig. 3. The 74F5074 $\overline{Q}$ output will not vary with respect to the Q trigger point even when the part is driven into a metastable state. Any tendency towards internal metastability is resolved by Signetics patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased Clock-to-Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the part defined by τ and T_o.

The metastability characteristics of the 74F5074 and related part types represent state-of-the art in TTL technology.
After determining the T_o and τ of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 74F50109 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the 74F50109 nanoseconds after the clock edge. He simply plugs his number into the equation below:

$$MTBF = e^{(t'/\tau)} / T_o f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t'>h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency or 20MHz because input events consist of both low and high data transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Fig. 4 it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula the actual MTBF is 1.51 x 10^{10} seconds or about 480 years.

MEAN TIME BETWEEN FAILURES (MTBF) versus t'

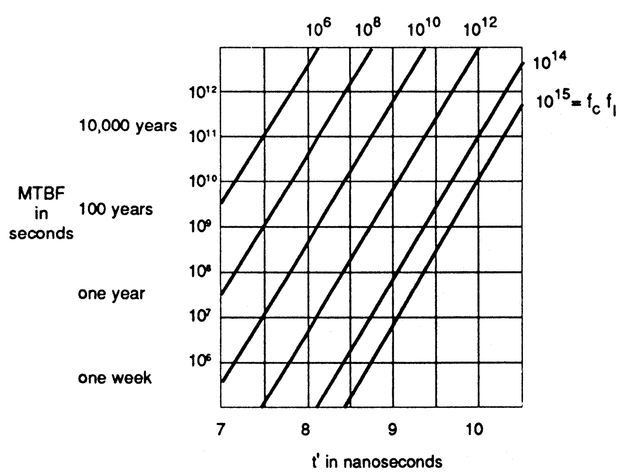
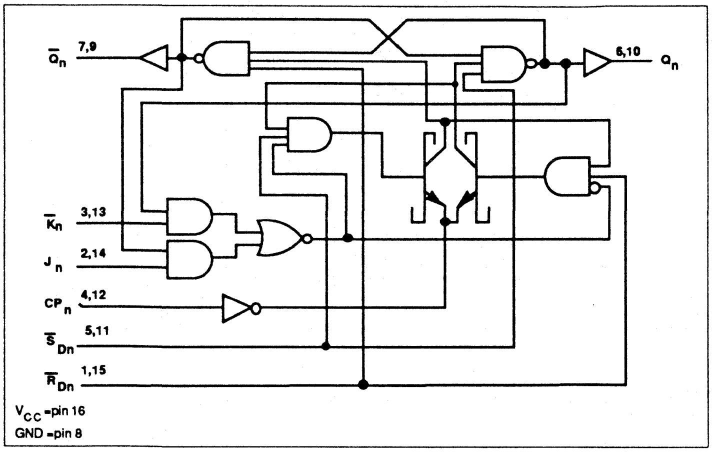


Fig. 4 MTBF versus t' for 74F50109 at τ = 135ps and T_o=9.8x 10^6 sec

Typical values for τ and T_o at various V_{CC}s and Temperatures

	0°C		25°C		70°C	
	τ	T_o	τ	T_o	τ	T_o
5.5 V	125 ps	1.0 x 10^9 sec	138 ps	5.4 x 10^6 sec	160 ps	1.7 x 10^5sec
5.0 V	115 ps	1.3 x 10^{10} sec	135 ps	9.8 x 10^6sec	167 ps	3.9 x 10^4 sec
4.5 V	115 ps	3.4 x 10^{13}sec	132 ps	5.1 x 10^8 sec	175 ps	7.3 x 10^4sec

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{S}_{Dn}$	$\overline{R}_{Dn}$	CP_n	J_n	$\overline{K}_n$	Q_n	$\overline{Q}_n$	
L	H	X	X	X	H	L	Asynchronous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H	H	Undetermined (Note)
H	H	↑	h	l	$\overline{q}$	q	Toggle
H	H	↑	l	l	L	H	Load "0" (Reset)
H	H	↑	h	h	H	L	Load "1" (Set)
H	H	↑	l	h	q	$\overline{q}$	Hold "no change"

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
q = Lower case indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Note = Both outputs will be High if both $\overline{S}_{Dn}$ and $\overline{R}_{Dn}$ go Low simultaneously.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the devicUnles otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS Min	LIMITS Nom	LIMITS Max	UNIT
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$V_{CC}\pm10\%$			-12	mA
		$V_{CC}\pm5\%$			-15	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} =-12mA	$\pm10\%V_{CC}$	2.5			V
					$\pm5\%V_{CC}$	2.7	3.4		V
				I_{OH} =-15mA	$\pm5\%V_{CC}$	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX	$\pm10\%V_{CC}$		0.30	0.50	V
					$\pm5\%V_{CC}$		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V					0.1	mA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	J_n, $\overline{K}_n$	V_{CC} =MAX, V_I = 0.5V					-250	μA
		CP_n, $\overline{S}_{Dn}$, $\overline{R}_{Dn}$						-20	μA
I_{OS}	Short circuit output current[3]		V_{CC} =MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} =MAX				22	32	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

AC ELECTRICAL CHARACTERISTICS

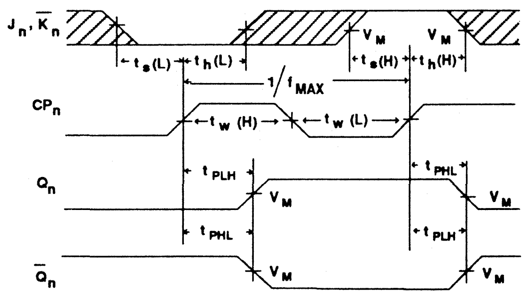
SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	130	150		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	3.8 3.8	6.0 6.0	2.0 2.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	3.5 3.5	5.5 5.5	8.0 8.0	3.0 3.0	8.5 8.5	ns
t_{PS}	Propagation delay Skew[1,3]	Waveform 4			1.0		1.0	ns
t_{OS}	Output to output Skew[2,3]	Waveform 4			1.5		1.5	ns

NOTE:
1. $| t_{PLH}$ actual - t_{PHL} actual $|$ for any output.
2. $| t_{PN}$ actual - t_{PM} actual $|$ for any output compared to any other output where N and M are either LH or HL.
3. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

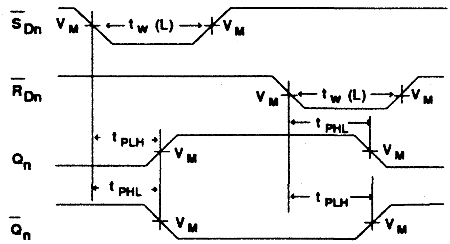
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n, $\overline{K}_n$ to CP_n	Waveform 1	1.5 1.5			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n, $\overline{K}_n$ to CP_n	Waveform 1	1.0 1.0			1.5 1.5		ns
$t_w(H)$ $t_w(L)$	CP_n Pulse width, High or Low	Waveform 1	3.0 4.0			3.5 5.0		ns
$t_w(L)$	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ Pulse width, Low	Waveform 2	3.5			4.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to CP_n	Waveform 3	3.0			3.5		ns

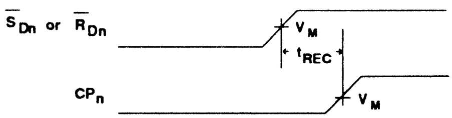
AC WAVEFORMS



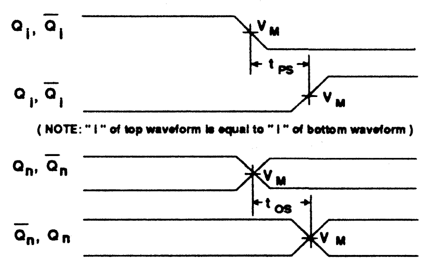
Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width



Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width



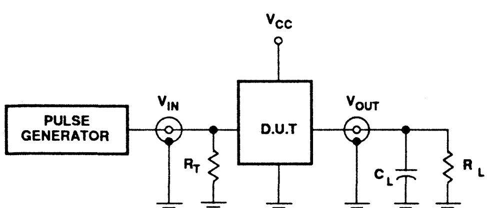
Waveform 3.
Recovery time for set or reset to clock



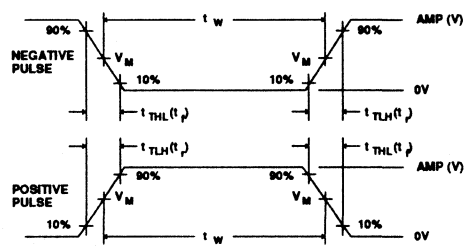
Waveform 4.
Propagation delay skew and output to output skew

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

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FAST Products	

74F50728
Flip-Flop

Synchronizing Cascaded Dual D-Type Flip-Flop With Metastable Immune Characteristics

FEATURES

- **Metastable Immune Characteristics**
- **Propagation delay skew and output to output skew less than 1.5ns**
- **See 74F5074 for Synchronizing Dual D-Type Flip-Flop**
- **See 74F50109 for Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop**
- **See 74F50729 for Synchronizing Dual D-Type Flip-Flop with Edge-Triggered Set and Reset**

DESCRIPTION

The 74F50728 is a cascaded dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

Set ($\overline{S}_{Dn}$) and Reset ($\overline{R}_{Dn}$) are asynchronous active-Low inputs and operate independently of the Clock (CP_n) input. They set and reset both flip-flops of a cascaded pair simultaneously. Data must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output. Data entering the 'F50728 requires two clock cycles to arrive at the outputs. The 'F50728 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50728 are: $\tau \cong$ 135ps and $T_0 \cong 9.8 \times 10^6$sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state .

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F50728	145 MHz	23mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F50728N
14-Pin Plastic SO	N74F50728D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/0.417	20µA/250µA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.033	20µA/20µA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/0.033	20µA/20µA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active Low)	1.0/0.033	20µA/20µA
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

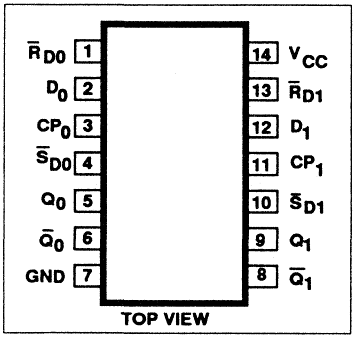
Synchronizing Solutions

Synchronizing incoming signals to a system clock has proven to be costly, either in terms of time delays or hardware. The reason for this is that in order to synchronize the signals a flip-flop must be used to 'capture' the incoming signal. While this is perhaps the only way to synchronize a signal, to this point, there have been problems with this method. Whenever the flop's setup or hold times are violated the flop can enter a metastable state causing the outputs in turn to glitch, oscillate, enter an intermediate state or change state in some abnormal fashion. Any of these conditions could be responsible for causing a system crash. To minimize this risk, flip-flops are often cascaded so that the input signal is captured on the first clock pulse and released on the second clock pulse (see Fig. 1). This gives the first flop about one clock period minus the flop delay and minus the second flop's clock-to-Q setup time to resolve any metastable condition. This method greatly reduces the probability of the outputs of the synchronizing device displaying an abnormal state but the tradeoff is that one clock cycle is lost to synchronize the incoming data and two separate flip-flops are required to produce the cascaded flop circuit. In order to assist the designer of synchronizing circuits, Signetics is offering the 74F50728. The 74F50728 consists of two pair of cascaded D-type flip-flops with metastable-immune features and is pin compatible with the 74F74. Because the flops are cascaded on a single part the metastability characteristics are greatly improved over using two separate flops that are cascaded. The pin compatibility with the 74F74 allows for plug-in retrofitting of previously designed systems.

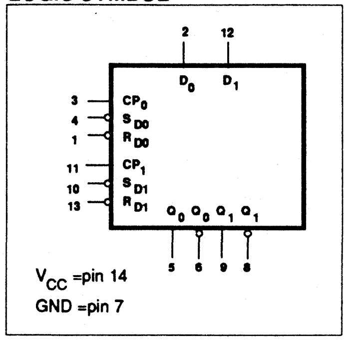
Because the probability of failure of the 74F50728 is so remote, the metastability characteristics of the part were empirically determined based on the characteristics of its sister part, the 74F5074. The table below shows the 74F5074 metastability characteristics.

Having determined the T_0 and τ of the flop, calculating the mean time between failures (MTBF) for the 74F50728 is simple. It is, however, somewhat different than calculating MTBF for a typical part because data requires two clock pulses to transit from the input to the output. Also, in this case a failure is considered any delay of the output beyond the nor-

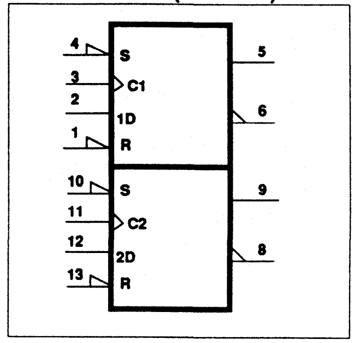
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



mal propagation delay. Suppose a designer wants to use the flop for synchronizing asynchronous data arriving at 10 MHz (as measured by a frequency counter) and is using a clock frequency of 50 MHz. He simply plugs his numbers into the equation below.

$$MTBF = e^{(t'/\tau)} / T_o f_C f_I$$

In this formula f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the period of the clock input (20 nanoseconds). In this situation the f_I will be twice the data frequency or 20 MHz because input events consist of both low and high data transitions. From Fig. 2 it is clear that the MTBF is greater than 10^{41} seconds. Using the above formula the actual MTBF is 2.23×10^{42} seconds or about 7×10^{34} years.

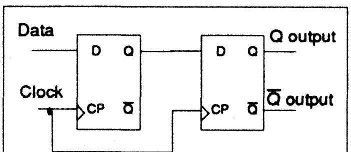


Fig. 1

Typical values for τ and T_o at various V_{CC}s and Temperatures

	0°C		25°C		70°C	
	τ	T_o	τ	T_o	τ	T_o
5.5 V	125 ps	1.0×10^{9} sec	138ps	5.4×10^{6}sec	160 ps	1.7×10^{5}sec
5.0 V	115ps	1.3×10^{10} sec	135 ps	9.8×10^{6}sec	167ps	3.9×10^{4}sec
4.5 V	115 ps	3.4×10^{13}sec	132ps	5.1×10^{8}sec	175 ps	7.3×10^{4}sec

Mean Time Between Failures versus Data Frequency at various Clock Frequency

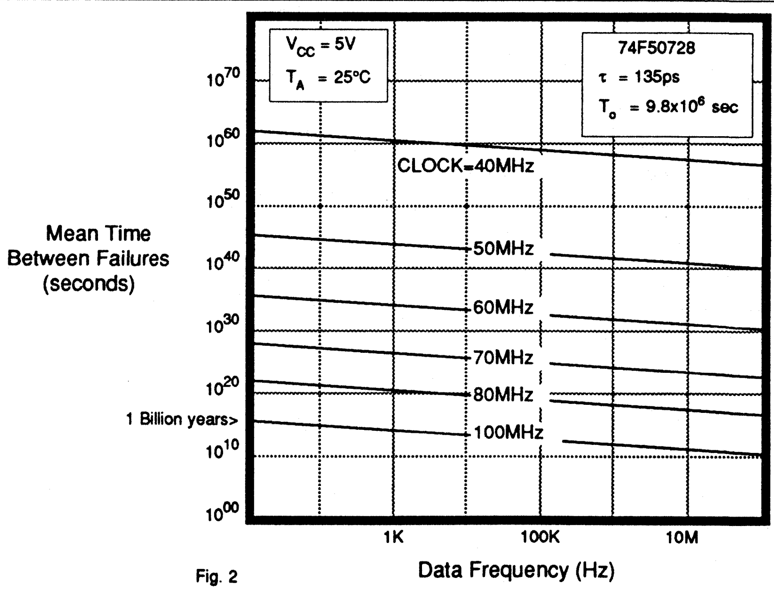
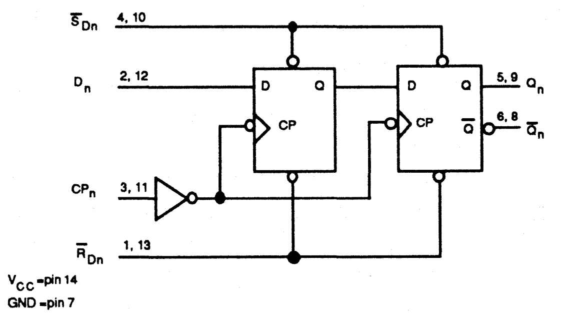


Fig. 2

Flip-Flop 74F50728

LOGIC DIAGRAM



FUNCTION TABLE(Note**)

INPUTS				INTERNAL REGISTER	OUTPUTS		OPERATING MODE
$\overline{S}_{Dn}$	$\overline{R}_{Dn}$	CP_n	D_n	Q	Q_n	$\overline{Q}_n$	
L	H	X	X	H	H	L	Asynchronous Set
H	L	X	X	L	L	H	Asynchronous Reset
L	L	X	X	X	H	H	Undetermined*
H	H	↑	h	h	H	L	Load "1"
H	H	↑	l	l	L	H	Load "0"
H	H	L	X	NC	NC	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
NC =No change from the previous setup
X = Don't care
* = This setup is unstable and will change when either Set or Reset return to the High level.
↑ = Low-to-High clock transition
** = Data entering the flop requires two clock cycles to arrive at the output (See Logic Diagram).

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS Min	LIMITS Nom	LIMITS Max	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	$\pm10\%V_{CC}$	2.5			V
					$\pm5\%V_{CC}$	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX	$\pm10\%V_{CC}$		0.30	0.50	V
					$\pm5\%V_{CC}$		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	D_n	V_{CC} = MAX, V_I = 0.5V					-250	µA
		$CP_n, \overline{S}_{Dn}, \overline{R}_{Dn}$						-20	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				23	34	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

AC ELECTRICAL CHARACTERISTICS

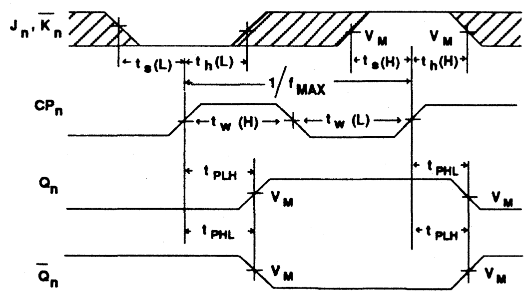
SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	145		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	3.8 3.8	6.0 6.0	1.5 2.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	3.5 3.5	5.0 5.0	8.0 8.0	3.0 3.0	9.0 8.5	ns
t_{PS}	Propagation delay Skew[1,3]	Waveform 4			1.0		1.0	ns
t_{OS}	Output to output Skew[2,3]	Waveform 4			1.5		1.5	ns

NOTE:
1. | t_{PLH} actual - t_{PHL} actual | for any one output.
2. | t_{PN} actual - t_{PM} actual | for any output compared to any other output where N and M are either LH or HL.
3. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

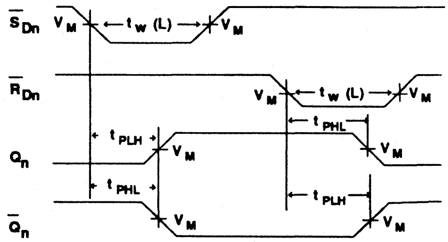
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP_n	Waveform 1	1.5 1.5			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP_n	Waveform 1	1.0 1.0			1.5 1.5		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 4.0			3.5 5.0		ns
$t_w(L)$	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to CP_n	Waveform 3	3.5			3.5		ns

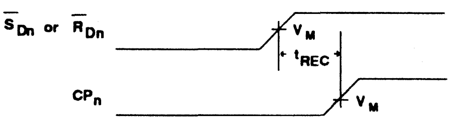
AC WAVEFORMS



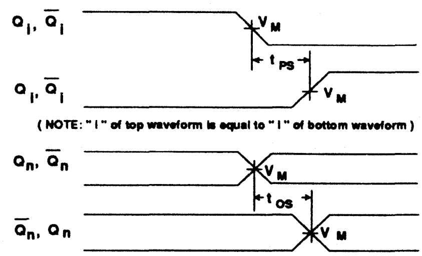
Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width



Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width



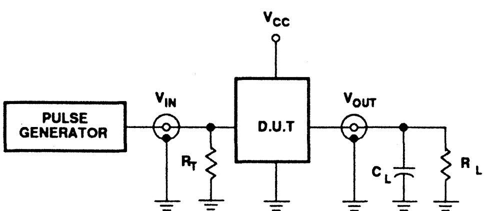
Waveform 3.
Recovery time for set or reset to clock



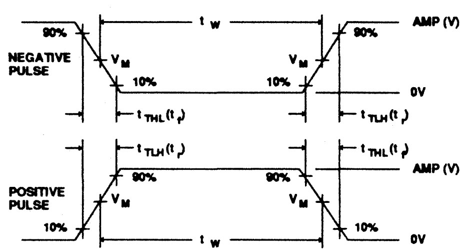
Waveform 4.
Propagation delay skew and output to output skew

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-1390
ECN No.	98904
Date of issue	February 23, 1990
Status	Product
FAST Products	

FAST 74F50729
Flip-Flop/Clock Driver

Synchronizing Dual D-Type Flip-Flop With-EdgeTriggered Set And Reset And Metastable Immune Characteristics

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F50729	120 MHz	19mA

FEATURES

- **Metastable Immune Characteristics**
- **Propagation delay skew and output to output skew guaranteed less than 1.5ns**
- **High source current (I_{OH}= 15mA) ideal for clock driver applications**
- **See 74F5074 for Synchronizing Dual D-Type Flip-Flop**
- **See 74F50109 for Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop**
- **See 74F50728 for Synchronizing Cascaded Dual D-Type Flip-Flop**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F50729N
14-Pin Plastic SO	N74F50729D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/0.417	20µA/250µA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.033	20µA/20µA
S_{D0}, S_{DI}	Set inputs (active rising edge)	1.0/0.033	20µA/20µA
R_{D0}, R_{DI}	Reset inputs (active rising edge)	1.0/0.033	20µA/20µA
Q_0, Q_I, $\overline{Q}_0$, $\overline{Q}_I$	Data outputs	750/33	15mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

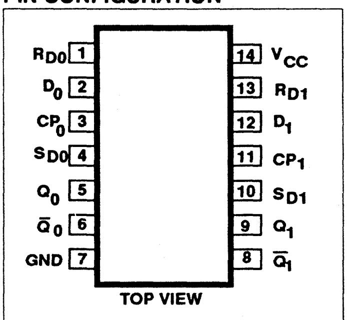
The 74F50729 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

Set (S_{Dn}) and Reset (R_{Dn}) are asynchronous positive-edge triggered inputs and operate independently of the Clock (CP_n) input. Data must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays.

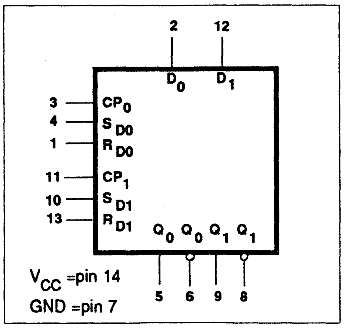
Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D_n input may be changed without affecting the levels of the output.

The 74F50729 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50729 are: $\tau \cong$ 135ps and $T_0 \cong 9.8 \times 10^6$sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state .

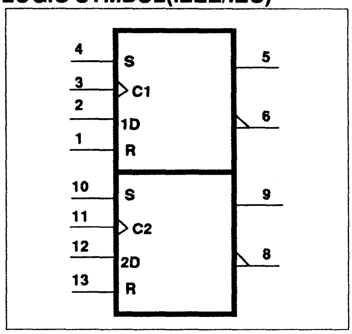
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Metastable Immune Characteristics

Signetics uses the term 'metastable immune' to describe characteristics of some of the products in its FAST family. Specifically the 74F50XXX family presently consists of 4 products which display metastable immune characteristics. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations. This claim is easily verified on the 74F5074. By running two independent signal generators (see Fig. 1) at nearly the same frequency (in this case 10 MHz clock and 10.02 MHz data) the device-under-test can often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

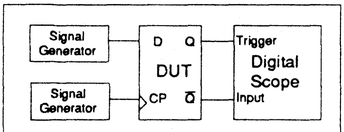


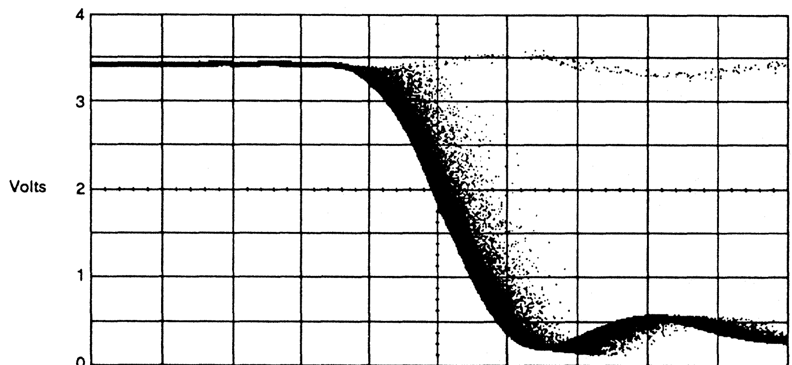
Fig. 1—Test Set up

When the device-under-test is a 74F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Fig. 2.

Fig. 2 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5 volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

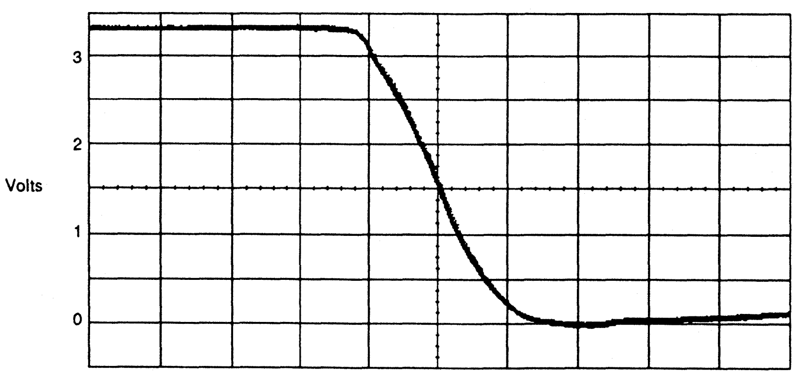
When the device-under-test is a metastable immune part, such as the 74F5074, the waveform will appear as in Fig. 3. The 74F5074 $\overline{Q}$ output will not vary with respect to the Q trigger point even when the part is driven into a metastable state. Any tendency towards internal metastability is resolved by Signetics patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased Clock-to-Q/$\overline{Q}$ propagation delay. This propagation delay is,

COMPARISON OF METASTABLE IMMUNE AND NON-IMMUNE CHARACTERISTICS



Time base = 2.00ns/div Trigger level = 1.5 Volts Trigger slope = positive

Fig. 2—74F74 $\overline{Q}$ output triggered by Q output, setup and hold times violated



Time base = 2.00ns/div Trigger level = 1.5 Volts Trigger slope = positive

Fig. 3—74F5074 $\overline{Q}$ output triggered by Q output, setup and hold times violated

of course, a function of the metastability characteristics of the part defined by τ and T_o.

The metastability characteristics of the 74F5074 and related part types represent state-of-the art in TTL technology.

After determining the T_o and τ of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the F50729 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz , and has decided that he would like to sample the output of the F50729 10 nanoseconds after the clock edge.

He simply plugs his numbers into the equation below:

$$MTBF = e^{(t'/\tau)} / T_o f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t'>h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency or 20MHz because input events consist of both low and high data transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Fig. 4 it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula the actual MTBF is 1.51×10^{10} seconds or about 480 years.

MEAN TIME BETWEEN FAILURES (MTBF) versus t'

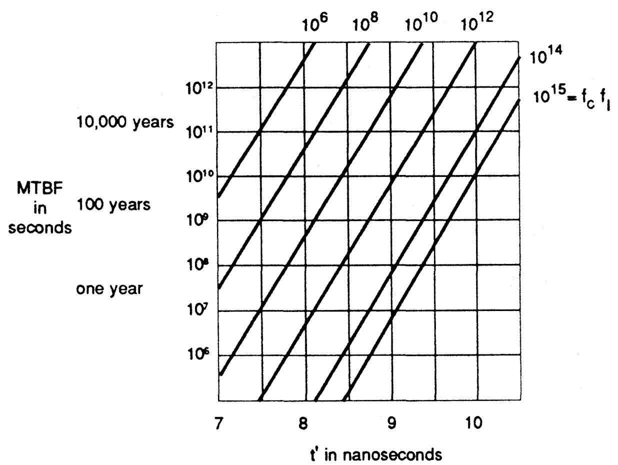
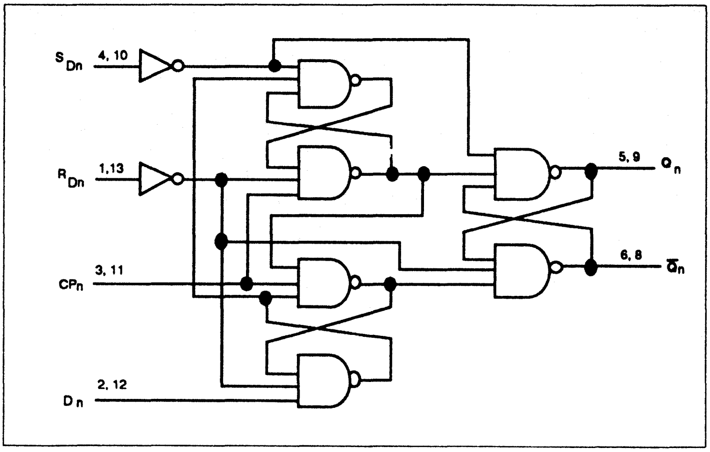


Fig. 4 MTBF versus t' for 74F50729 at τ = 135ps and T_o=9.8x 10^6 sec

Typical values for τ and T_o at various V_{CC}s and Temperatures

	0°C		25°C		70°C	
	τ	T_o	τ	T_o	τ	T_o
5.5 V	125 ps	1.0×10^9 sec	138ps	5.4×10^6 sec	160 ps	1.7×10^5sec
5.0 V	115ps	1.3×10^{10} sec	135 ps	9.8×10^6sec	167ps	3.9×10^4 sec
4.5 V	115 ps	3.4×10^{13}sec	132ps	5.1×10^8 sec	175 ps	7.3×10^4sec

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
S_D	R_D	CP	D	Q	$\overline{Q}$	
$\uparrow$	$\not\uparrow$	X	X	H	L	Asynchronous Set
$\not\uparrow$	$\uparrow$	X	X	L	H	Asynchronous Reset
$\not\uparrow$	$\not\uparrow$	$\uparrow$	h	H	L	Load "1"
$\not\uparrow$	$\not\uparrow$	$\uparrow$	l	L	H	Load "0"
$\not\uparrow$	$\not\uparrow$	$\not\uparrow$	X	NC	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care
$\uparrow$ = Low-to-High transition
NC = No change from the previous setup
$\not\uparrow$ = Not Low-to-High transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS Min	LIMITS Nom	LIMITS Max	UNIT
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$V_{CC}\pm10\%$			-12	mA
		$V_{CC}\pm5\%$			-15	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -12mA	$\pm10\%V_{CC}$	2.5			V
					$\pm5\%V_{CC}$	2.7	3.4		V
				I_{OH} = -15mA	$\pm5\%V_{CC}$	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX	$\pm10\%V_{CC}$		0.30	0.50	V
					$\pm5\%V_{CC}$		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	D_n	V_{CC} = MAX, V_I = 0.5V					-250	μA
		CP_n, S_{Dn}, R_{Dn}						-20	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				19	27	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

AC ELECTRICAL CHARACTERISTICS

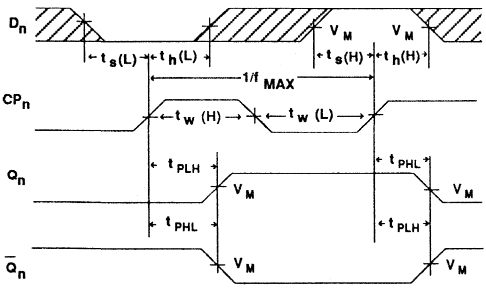
SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	120		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	3.9 3.9	6.0 6.0	1.5 2.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay S_{Dn}, R_{Dn} to Q_n or $\overline{Q}_n$	Waveform 2	2.0 3.0	4.0 5.0	6.5 7.5	1.5 2.0	7.5 8.0	ns
t_{PS}	Propagation delay Skew[1,3]	Waveform 4			1.0		1.0	ns
t_{OS}	Output to output Skew[2,3]	Waveform 4			1.5		1.5	ns

NOTE:
1. | t_{PLH} actual - t_{PHL} actual | for any output.
2. | t_{PN} actual - t_{PM} actual | for any output compared to any other output where N and M are either LH or HL.
3. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

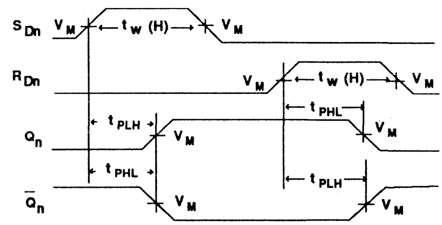
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP_n	Waveform 1	1.5 1.5			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP_n	Waveform 1	1.0 1.0			1.5 1.5		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 4.0			3.5 6.0		ns
$t_w(H)$	S_{Dn} or R_{Dn} Pulse width, High	Waveform 2	3.5			4.0		ns
t_{REC}	Recovery time S_{Dn} or R_{Dn} to CP_n	Waveform 3	6.0			6.5		ns
t_{REC}	Recovery time S_{Dn} to R_{Dn} or R_{Dn} to S_{Dn}	Waveform 3	1.0			1.0		ns

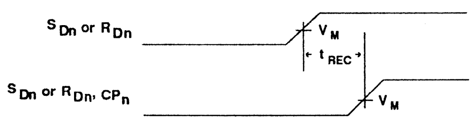
AC WAVEFORMS



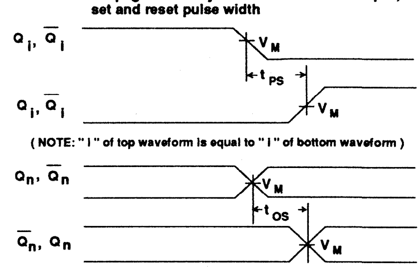
Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width



Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width



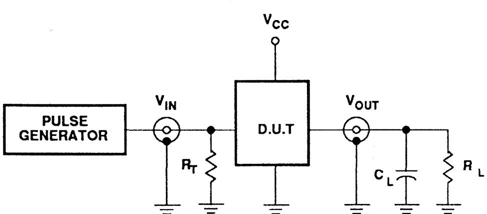
Waveform 3.
Recovery time for set or reset to clock and set to reset or reset to set



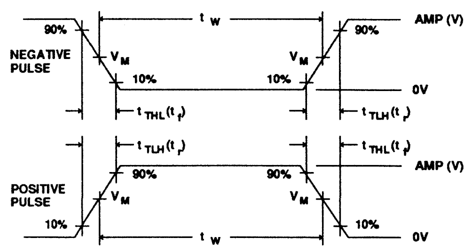
Waveform 4.
Propagation delay skew and output to output skew

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST application notes

AN219
A Metastability Primer

Application Note

Standard Products

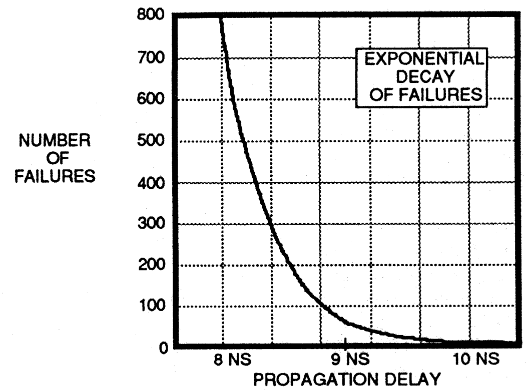


Figure 1

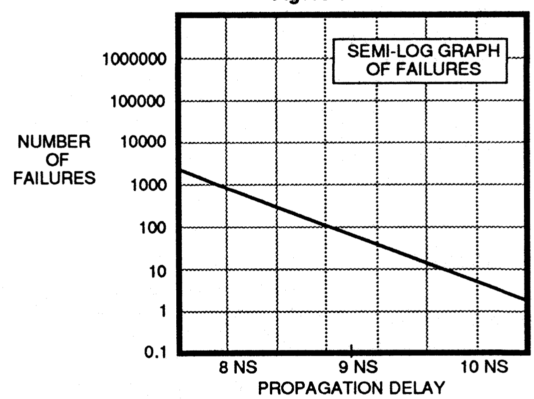


Figure 2

INTRODUCTION

When using a latch or flip-flop in normal circumstances (i.e. when the device's setup and hold times are not being violated) the outputs will respond to a latch enable or clock pulse within some specified time. These are the propagation delays found in the data sheets. If, however, the setup and hold times are violated so that the data input is not a clear one or zero, there is a finite chance that the flip-flop will not immediately latch a high or low but get caught half way in between. This is the metastable state and it is manifested in a bi-stable device by the outputs glitching, going into an undefined state somewhere between a high and low, oscillating, or by the output transition being delayed for an indeterminable time.

Once the flip-flop has entered the metastable state, the probability that it will still be metastable some time later has been shown to be an exponentially decreasing function. Because of this property, a designer can simply wait for some added time after the specified propagation delay before sampling the flip-flop output so that he can be assured that the likelihood of metastable failure is remote enough to be tolerable. On the other hand one consequence of this is that there is some probability (albeit vanishingly small) that the device will remain in a metastable state forever. The designer needs to know the characteristics of metastability so that he can determine how long he must wait to achieve his design goals.

THE CHARACTERISTICS OF METASTABILITY

In order to define the metastability characteristics of a device three things must be known: first, what is the likelihood that the device will enter a metastable state? This propensity is defined by the parameter 'T_0'. Second, once the device is in a metastable state how long would it be expected to remain in that state? This parameter is tau (τ) and is simply the exponential time constant of the decay rate of the metastability. It is sometimes called the metastability time constant. The final parameter is the measured propagation delay of the device. Commonly, the typical propagation delays found in the data book are used for this and it is designated 'h' in the equations (although most designers are familiar with this value as Tpd). Now let's see how tau and T_0 are determined by measurements.

A TEST METHOD

Suppose we wanted to measure the metastability characteristics of a fictitious edge-triggered D-type flip-flop and we had a test system that would count each time the flip-flop is found in a metastable state at some time after a clocking edge. The first thing we would like to know about the flip-flop would be the h or typical propagation delay. We could measure the delay or look it up in the data book (of course, measuring the actual delay would allow more precise results). This fictitious flip-flop has an h of 7 ns. In this test we decide to use a clock frequency of 10 MHz. This frequency is primarily a function of the test systems ability to assimilate the information. The data will run at 5 MHz asynchronously to the clock and with a varying period. This frequency was chosen because at two transitions per cycle the data signal produces 10 million points each second where it is possible for the flip-flop to go into a metastable state, an average of one point for each clock pulse. An important point about the characteristic of the data signal in relation to the clock is that the data transitions must have an equal probability of occurring anywhere within the clock period or the results could be skewed. In other words, we need to have a uniform distribution of random data transitions (high and low) relative to the clocking edge.

The first measurement we take is to determine the number of times the device is still in a metastable state 8 ns after the clock edge. With this device there are 792 failures after 1 billion clock cycles. Changing the time to 9 ns we measure 65 failures after another 1 billion cycles. Because metastability resolves as an exponentially decaying function the two points define the exponential curve and they can be plotted as shown in Figure 1. An equivalent plot can be made using a semilog scale as in Figure 2. The slope of the line drawn through the two points represents tau. With these two points the tau can be determined by equation (1):

$$(1)\quad \tau = \frac{t_2 - t_1}{ln(N_1 / N_2)}$$

where N_1 and N_2 are the number of failures at times t_1 and t_2, respectively.

Working thru the numbers gives us a tau of 0.40 ns. Tau of this order is representative of the FAST line of flip-flops.

Earlier we stated that T_0 is an indicator of the likelihood that the device will enter a metastable state. Now we will attempt to explain it. At 9 ns after the clock we observed 65 failures in 1 billion clock cycles. Since the data transits on average once per clock cycle and the period of this clock is 100 ns, from equation (2) we can say that there appears to be an aperture about 0.0065 picoseconds wide at the input of the device that allows metastability to occur for 9 or more nanoseconds. Another way of explaining the same thing would be to suppose that if 1 billion data

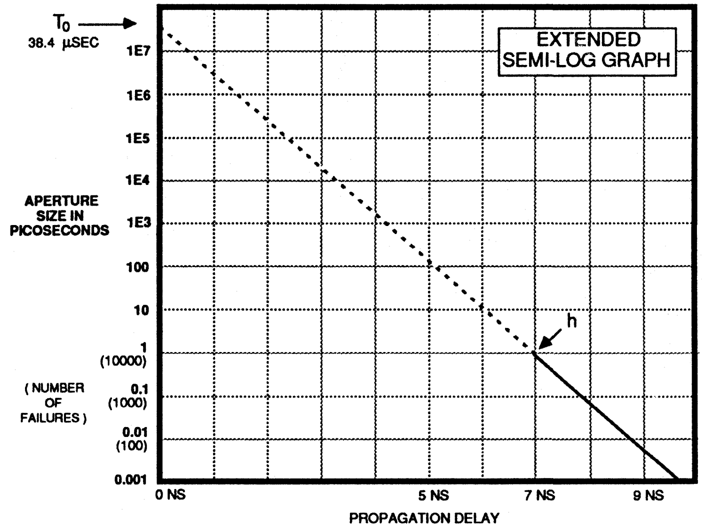


Figure 3

transitions were uniformly and randomly distributed over a clock period of 100 ns: you would expect 65 of these transitions to cause the outputs to go into a metastable state and remain there for at least 9 ns.

$$(2)\quad T_9 = \frac{N_9 P_C}{N_{C9}}$$

Where N_{C9} is the number of clocking events at 9 ns (in this instance, 1 billion), P_C is the period of the clock, and N_9 is the number of failures recorded at 9 ns.

By the same reasoning the window at 8 ns appears to be 0.0792 picoseconds wide. It seems to have grown because there are, of course, more failures after 8 ns than after 9 ns. This aperture has been normalized by researchers to indicate the effective size of the aperture at the clock edge, or time zero. Unfortunately the normalization process tends to obscure the interpretation of T_0. T_0 can be calculated using equation (3). Figure 3 is an extension of Figure 2 and shows the relationship of T_0, h, and tau.

$$(3)\quad T_0 = T_8 e^{\left(\frac{8ns}{\tau}\right)}$$

or equivalently,

$$T_0 = T_9 e^{\left(\frac{9ns}{\tau}\right)}$$

In this case T_0 is 38.4 microseconds and this value is again typical of the FAST line of products.

Figure 3 is an extension of Figure 2 and gives a graphic indication of T_0. The number of failures plots on the same scale as the aperture size but the number of failures is dependent on the number of clock cycles used in the test (we always used 1 billion in this paper) and the ratio of data transitions to clock pulses (1:1 in this paper). On the other hand, the aperture size is independent of these things.

MTBF

Having determined the T_0 and tau of the flip-flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the flip-flop for synchronizing asynchronous data that is arriving at 10 MHz, he has a clock frequency of 25 MHz, and has decided that he would like to sample the output of the flip-flop 15 ns after the clock edge. He simply plugs his numbers into equation (4).

$$(4)\quad MTBF = \frac{e^{\left(\frac{t'}{\tau}\right)}}{T_0 f_C f_i}$$

In this formula f_C is the frequency of the clock, f_i is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (of course t'>h). In this situation the f_i will be twice the data frequency because input events consist of both low and high data transitions. For the numbers above the MTBF is one million seconds or about one failure every 11.6 days. If the designer would have tried to sample the data after only 10 ns the MTBF would have been 3.8 seconds.

Metastability literature can be very confusing because several companies use different nomenclature and often the fundamental parameters are obscured by scale factors, so it is important that the user understand MTBF. Let's try a thought experiment to determine the correct MTBF formula. We know the size of the aperture at 8 ns so we need to know how often that window will occur. This is supplied by the clock period. This gives a ratio of window size to clock period and gives us the likelihood of a transition within the clock period causing a metastable state that lasts beyond the 8 ns point. Now we need to know the number of input events per clock period to determine the MTBF at 8 ns. This is supplied by the average input event period and produces the equation below where P_C and P_i are the periods of the clock and input events, respectively.

$$(5)\quad MTBF = \frac{1}{T_8 \frac{1}{P_C}\frac{1}{P_i}} = \frac{1}{T_8 f_C f_i}$$

This gives the MTBF for 8 ns, but how can the formula be developed to handle other times? It has been stated in this paper that the rate of decay of metastable events is an exponential function with a time constant of tau. Using this information gives the equation below where t' is the time after the clock pulse that the output is sampled.

$$(6)\quad MTBF = \frac{e^{\left(\frac{t'-8ns}{\tau}\right)}}{T_8 f_C f_i} = \frac{e^{\left(\frac{t'}{\tau}\right)}}{T_8 e^{\left(\frac{8ns}{\tau}\right)} f_C f_i}$$

$$= \frac{e^{\left(\frac{t'}{\tau}\right)}}{T_0 f_C f_i}$$

A point should be made here about MTBF. This is the mean time between failures and as such does not indicate the average time between failures. In fact, in this situation, the MTBF is the time before which there is a 63.2% probability that a failure would have occurred. Suppose a device has an MTBF of one million seconds like the example above; because the MTBF is an exponential function there is a 9.5% probability that a failure will occur in the first 1.16 days of operation. This might cause the user to feel that the device is failing more than expected. The user would find that 50% of his failures would occur within 8 days. Figure 4 gives a visual interpretation of this idea: time constant one represents one million seconds in this case.

RECENT DEVELOPMENTS

The quest for better metastability characteristics in flip-flops has recently resulted in the development of flip-flops with taus significantly less than 0.40 ns. Perhaps the most notable of these is the Signetics 74F50XXX series with typical taus of 135 ps. The specifications of these new products can cause confusion among the uninitiated because the typical T_0 on these devices is 9.8 million seconds or about 113 days. This is an example of how the normalization process obscures the interpretation of T_0. In the newest products the taus have decreased faster than the normal propagation delays primarily due to speed limitations of the outputs.

Using the example above and calculating T_7 from equation (3) we see that the window at h is 0.965 ps. Now let's assume that we have a device with the same size window (0.965 ps) at h and an h of 7 ns. The difference between this device and the previous example is that this device has a tau of 150 ps. Clearly, if the device has the same h and the same size of window at h but a smaller tau, the device is better. But let's calculate the T_0.

$$T_0 = T_7 e^{\left(\frac{7ns}{\tau}\right)}$$

T_0=178 million seconds!

Comparing the T_0 of any two devices does not show which device is superior. However, one can expect that the device with the lower tau is superior in all but the most peculiar circumstances.

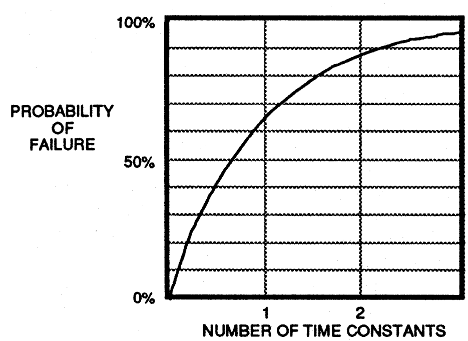


Figure 4

Standard Products

AN220

Synchronizing and Clock Driving Solutions—Using the 74F50XXX Family

Application Note

THE 74F50XXX FAMILY

- **74F5074 Synchronizing Dual D-Type Flip-Flop**
- **74F50728 Synchronizing Cascaded D-Type Flip-Flop**
- **74F50729 Synchronizing Dual D-Type Flip-Flop with Edge-Triggered Set and Reset**
- **74F50109 Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop**

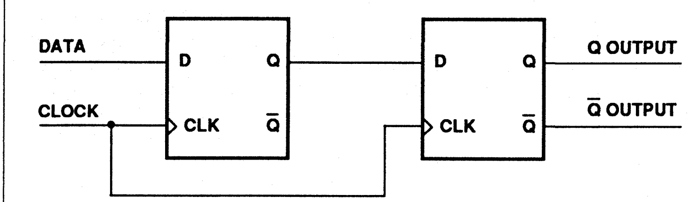


Figure 1 — Cascaded Flip-Flops

MAJOR FAMILY FEATURES

- **Metastable immune characteristics**
- **Propagation delay skew and output to output skew guaranteed to be less than 1.5ns**
- **Balanced output currents for clock driver applications ($I_{OH} = I_{OL}$ = 20mA)**

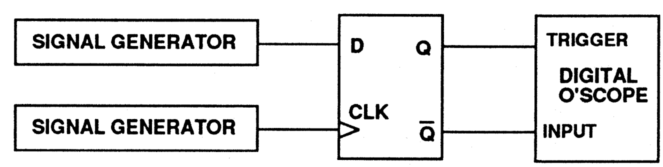


Figure 2—Test Setup

INTRODUCTION

Philips 74F50XXX series of products have been designed to resolve synchronization problems and at the same time produce complementary metastable/ immune outputs with remarkably small skews useful in clock driving applications. The 74F5074 and 74F50109 are pin and function compatible replacements of the 74F74 and 74F109 respectively. The 74F50728 consists of two pair of cascaded D-type flip-flops, and the 74F50729 is a pin compatible replacement for the 74F74 with edge-triggered set and reset inputs.

SYNCHRONIZATION

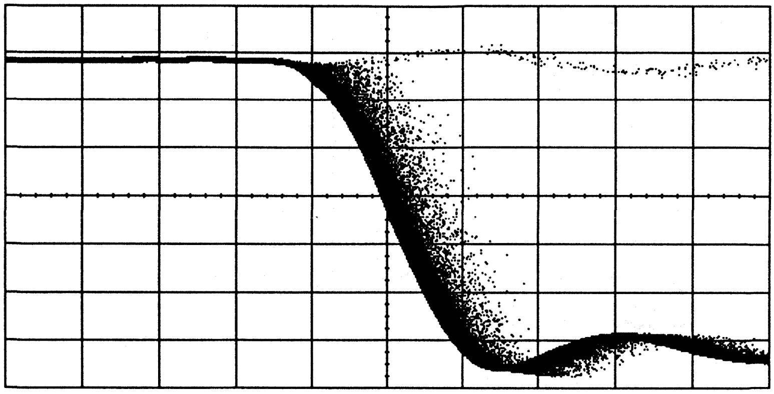
Synchronizing incoming signals to a system clock has proven to be costly, either in terms of time delays or hardware. In order to synchronize a signal a flip-flop is normally used to 'capture' the incoming signal. When a flip-flop is used in this mode its setup and hold times are occasionally violated. Whenever this occurs the flip-flop can enter a metastable state causing the outputs to glitch, oscillate, enter an intermediate state or change state in some abnormal fashion. Any of these conditions could cause a system to crash. To minimize this risk, flip-flops are often cascaded so that the input signal is captured on the first clock pulse and released on the second clock pulse (see Figure 1). This gives the first flip-flop about one clock period minus its propagation delay and minus the second flip-flop's clock-to-Q setup time to resolve any metastable condition. This method greatly reduces the probability that the outputs of the synchronizing device may display an abnormal state, but the trade-off is that one clock cycle is lost to synchronize the incoming signal. Often two separate flip-flop packages are required to produce the cascaded flip-flop circuit.

The 74F50XXX series of products have five design features that cause them to be immune from metastability problems. First, the flip-flops are designed so that their outputs cannot change state until any internal metastability has been resolved. This assures that the outputs will not glitch, oscillate, enter an intermediate state, or change state in some abnormal fashion. Second, the setup and hold time window has been minimized to reduce the likelihood of internal flip-flops entering a metastable state. Third, the internal flip-flops have specifically been designed to exit a metastable state as rapidly as possible. Fourth, the Clock-to-Q propagation delays through the part have been made as short as possible. Finally, Philips has used the best oxide-isolated process available to make these products the best synchronization solutions possible.

METASTABLE IMMUNITY

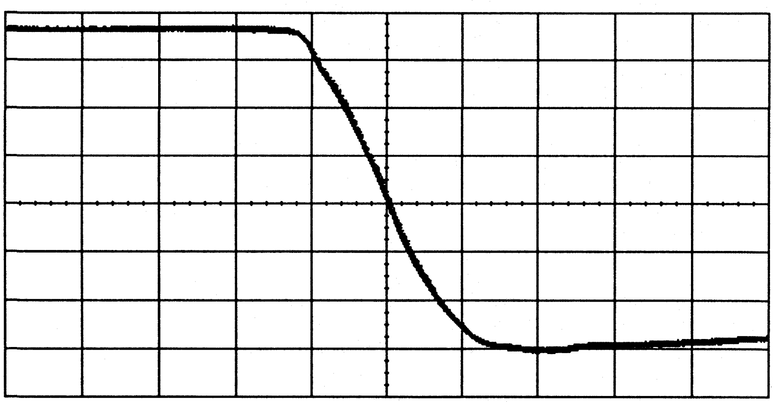
Philips uses the term 'metastable immune' to describe characteristics of some of the products in its FAST family, specifically the 74F50XXX family which presently consists of 4 products. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations. This claim is easily verified on the 74F5074.

When a test is performed (see Figure 2) where two independent signal generators are running at nearly the same frequency (in this case 10 MHz clock and



Timebase= 2.00 ns/div
Offset = 2.0Volts
Trigger level = 1.5 Volts
Trigger slope = positive

Figure 3—74F74 $\overline{Q}$ Output Triggered By Q Output, Setup And Hold Times Violated



Timebase = 2.00 ns/div
Offset = 1.5 Volts
Trigger level = 1.5 Volts
Trigger slope = positive

Figure 4—74F5074 $\overline{Q}$ Output Triggered By Q Output, Setup And Hold Times Violated

10.02 MHz data) the device-under-test operates continuously in the region where metastability can occur. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform.

When the device-under-test is a 74F74 (which was not designed with metastable immune characteristics) the waveform appears as shown in Figure 3. This figure clearly shows that the Q output can vary in time with respect to the Q trigger point. It also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a micro-channel plate CRT. Perhaps of even greater interest are the dots running along the 3.5 volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

When the device-under-test is a metastable immune part, such as the 74F5074, the waveform appears as shown in Figure 4. The 74F5074 $\overline{Q}$ output does not vary with respect to the Q trigger point even when the part is driven into a metastable state. Any tendency towards internal metastability is resolved by Signetics patented circuitry. If a metastable event occurs within the flip-flop the only outward manifestation of the event will be an increased Clock-to-Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the device (see below).

METASTABILITY CHARACTERISTICS

In order to define the metastability characteristics of these products Philips

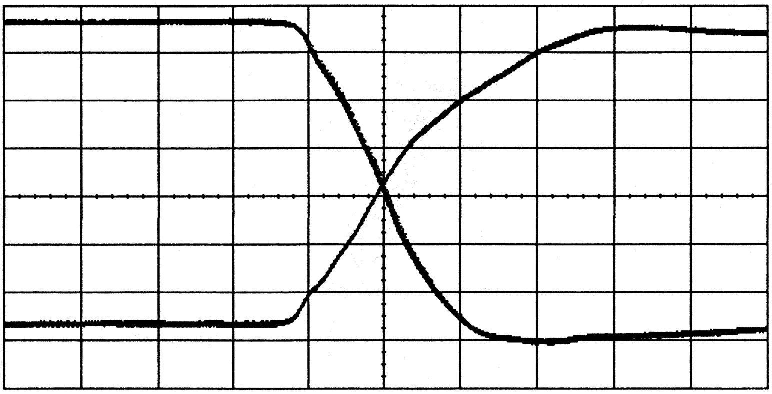


Figure 5—74F5074 $\underline{Q}$ And Q Outputs Skew Relationship At 5 Volts V_{CC} And Room Temperature

has chosen to use the parameters described by Thomas J. Chaney and Fred U. Rosenberger of Washington University in St. Louis, Missouri in their paper "Characterization and Scaling of MOS Flip-flop Performance in Synchronous Applications" in the *Proceedings of the Caltech Conference on VLSI*, January 1979. These parameters were chosen because they are fundamental and the best papers written on metastability use these parameters.

The first parameter to be considered is T_0. T_0 is a function of the propensity of a latch to enter a metastable state. It is also a very strong function of the normal propagation delay of the device and is generally given in units of seconds. The second parameter is h. It is the propagation delay from Clock-to-Q through a device under normal (i.e., no internal metastability) operation. The final parameter is tau (τ). Tau is the exponential time constant of the rate at which a latch in a metastable state resolves that condition and is typically specified in tenths of nanoseconds. Tau is generally the most important of the defining parameters.

To determine the Mean Time Between Failures (MTBF) the following formula is used:

$$\text{MTBF} = \frac{\left[\exp\left(\frac{t'}{\tau}\right)\right]}{\left[T_0\,(\text{clock rate})(\text{input data rate})\right]}$$

where t' is the time given between the flip-flop clock and the output sampling time. This time is always greater than h. One point to keep in mind is that the input data rate is twice the frequency of the input signal because each cycle of the pulse generator produces two data inputs, one high and one low. A pulse generator operating at 5 MHz produces an input data rate of 10 MHz.

As an example using the 74F5074, assume that one failure per century is acceptable and both data and the clock are at 10 MHz. A typical tau for the 54F5074 is 135 picoseconds with a T_0 of 9.8E6 seconds. Since one century equals about three billion seconds, substituting into the equation above gives:

$$3\text{E}9\ \text{sec} = \frac{\left[\exp\left(\frac{t'}{0.135\ \text{ns}}\right)\right]}{\left[9.8\text{E}6(10\ \text{MHz})(10\ \text{MHz})\right]}$$

$$t' = 9.5\ \text{ns}$$

If an additional nanosecond were allowed between the clock and the sampling point one could expect a failure about once every 1.7 million years.

The 74F728 MTBF can be determined by setting the clock period to the t' so that in the example above the t'=100 ns. This t' gives:

$$\text{MTBF} = \frac{\left[\exp\left(\frac{100\ \text{ns}}{0.135\ \text{ns}}\right)\right]}{\left[9.8\text{E}6(10\ \text{MHz})(10\ \text{MHz})\right]}$$

$$\text{MTBF} = 5.0\text{E}321\ \text{seconds}$$

or 1.6E312 centuries!

Note that in this case a failure is considered to be any propagation delay beyond the delay expected in a situation where setup and hold times were not violated. Assuming data and clock rates of 100 MHz gives:

$$\text{MTBF} = \frac{\left[\exp\left(\frac{10\ \text{ns}}{0.135\ \text{ns}}\right)\right]}{\left[9.8\text{E}6(100\ \text{MHz})(100\ \text{MHz})\right]}$$

$$\text{MTBF} = 1.5\text{E}9\ \text{seconds}$$

or 48 years!

SKEW CHARACTERISTICS

One of the requirements for an effective clock driver is that the complementary outputs have a small skew relative to each other. Figure 5 shows a picture of the 74F5074 outputs at room temperature with a 5 volt V_{CC}. Because of Philips patented circuitry the output skews will always remain tightly coupled over temperature and V_{CC}.

SUMMARY

Because of their minimum output skews, metastable immune characteristics, and balanced output drive capabilities the

Synchronizing and Clock Driving Solutions—Using the 74F50XXX Family

AN220

74F50XXX series of products offer viable solutions to synchronization and clock driver problems.

Document No.	Application Note
ECN No.	
Date of issue	January, 1990
Status	
FAST Products	

AN221
Multiplying and Dividing Clock Frequencies Using the 74F50729

INTRODUCTION

Subtle differences in a device's design sometimes allow unusual applications. Consider the difference between edge triggered and level sensitive inputs—

SINGLE 14-PIN IC DOUBLES INPUT FREQUENCY

The 74F50729 from Philips is a dual D-type flip-flop. The part is functionally equivalent to the 74F74 except that set and reset are positive edge triggered rather than level sensitive. The circuits described in this application note make use of the edge triggered set and reset features of the 74F50729. The first circuit is a frequency doubler. It is shown in Figure 1a along with input and output waveforms running at 30MHz and 60MHz respectively (Figure 1b).

The operation of the frequency doubler is as follows. When the flip-flop starts out in the high state, the first rising clock edge will toggle the flip-flop into the low state because the Q' is tied back to D. From here each rising clock or clock' edge will toggle the part into the high state, and this rising edge will trigger the CLR input to put the part back into the low state. Since each transition on the input clock produces two transitions at the output, the output frequency is twice that of the input. The width of the high going pulses can be increased by placing a delay in the path of the CLR signal.

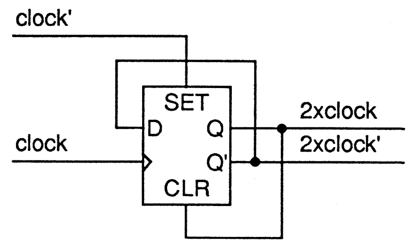


Figure 1a. Frequency doubler

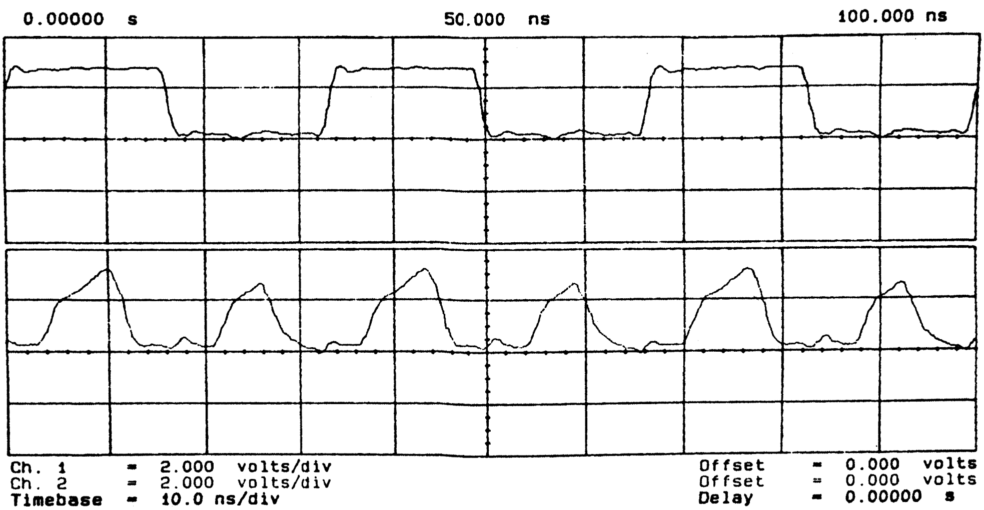


Figure 1b. Input (top) and output (bottom) waveforms from a 2X frequency multiplier

MULTIPLY INPUT FREQUENCY BY N USING N FLIP-FLOPS

The 74F50729 can also be used to multiply input frequencies by n using n flip-flops. The circuit shown in Figure 2a uses n flip-flops to produce a series of n pulses in response to each rising transition at the input. The pulse width high and low can be independently increased by increasing the delays shown in Figure 2b.

To understand the operation of this circuit, imagine $Q_{1..n}$ starting out in the low state and $Q'_{1..n}$ in the high state. A low to high transition at the $CLK_{1..n}$ inputs will cause $Q_{1..n}$ to go high and $Q'_{1..n}$ to go low. The low to high transitions of $Q_{1..n}$ will trigger the $CLR_{1..n}$ inputs bringing $Q_{1..n}$ back low and $Q'_{1..n}$ back high. The low to high transitions of $Q'_{1..n-1}$ will trigger $SET_{2..n}$ putting $Q_{2..n}$ into the high state and $Q_{2..n}$ into the low state. The low to high transitions of $Q_{2..n}$ will again trigger the $CLR_{2..n}$ inputs bringing $Q_{2..n}$ back low and $Q'_{2..n}$ back high. This in turn will stimulate another set of pulses on $Q_{3..n}/Q'_{3..n}$ stimulating another set on $Q_{4..n}/Q'_{4..n}$ and so on. When the sequence is complete, Q_n will have produced n rising pulses, Q_{n-1} will have produced n-1 rising pulses, and so on down through Q_1 which will have produced one pulse.

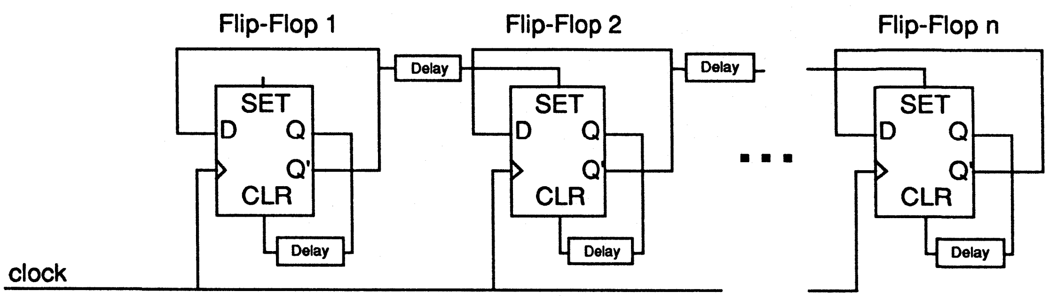


Figure 2a. Multiply by n

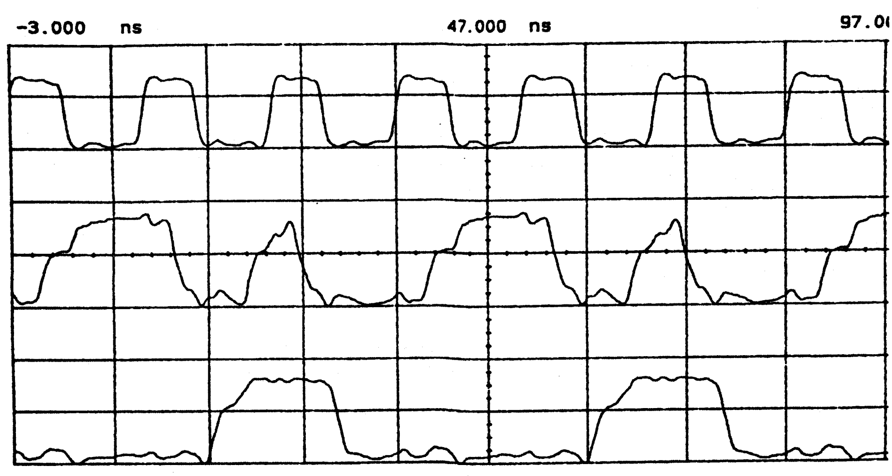


Figure 2b. Input and output waveforms from a 4X frequency multiplier. The waveforms are (in descending order) Clock, Clock2, Clock 3, and Clock4.

DIVIDING THE INPUT FREQUENCY BY 1.5 AND 3

The final circuit in Figure 3a works much like a two bit ripple counter except that it increments itself from the count of two to the count of three without requiring an input clock edge. To trace through the circuit operation, imagine the two flip-flops both starting out in the low state (see Figure 3b). The first rising clock edge will toggle flip-flop 1 into the high state. The next rising clock edge will toggle flip-flop 1 into the low state which will toggle flip-flop 2 into the high state which will trigger the SET input of flip-flop putting it back into the high state. The next rising clock edge will toggle flip-flop 1 into the low state which will toggle flip-flop 2 into the low state. The two flip-flops have wrapped back around to their initial state and it has taken three input clock cycles. In three input clock cycles flip-flop 1 goes through the repetitive sequence 0101 (two full cycles), so its output frequency is two thirds or 1/1.5 that of the input. In three input clock cycles flip-flop 2 has gone through the repetitive sequence 0011 (one full cycle), so its output frequency is one third that of the input.

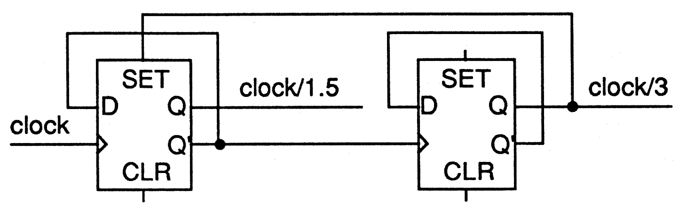


Figure 3a. Divide by 1.5 and 3

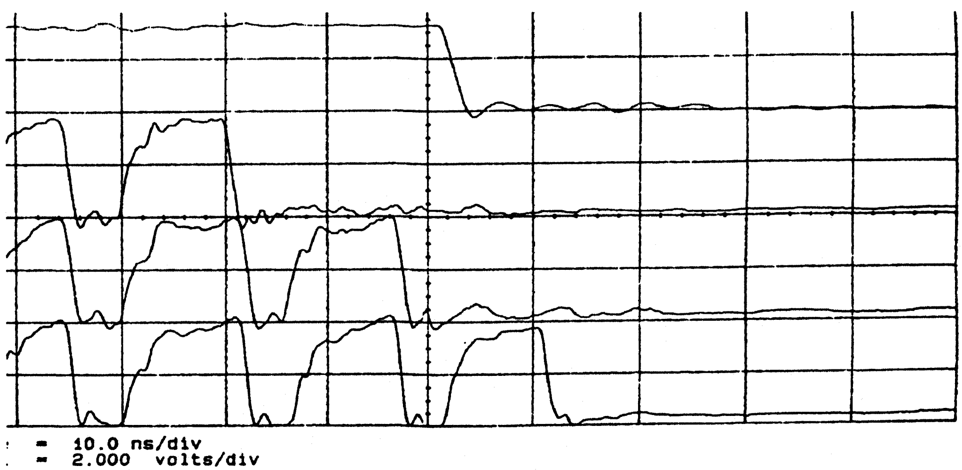


Figure 3b. Input and output waveforms from a 1.5 and 3 frequency divider. The waveforms are (in descending order) Clock, Clock/1.5, and Clock/3.

AN222

Eliminating Glitches—Using the 74F50XXX Family

Application Note

Standard Products

INTRODUCTION

One of the hazards of using self-timed circuits is that, on occasion, a glitch or runt pulse can appear because of race conditions. Because this pulse is too small to be interpreted as a legitimate one or zero, it can wreak havoc with a design.

A SOLUTION

The following circuits turn runt pulses into useable fixed width pulses or, if the input is too small, block the input. This idea is especially useful if the output is being used to trigger a set, reset, or clock input of another flip-flop.

Figure 1 shows half of a Philips 74F5074 in a configuration that will turn a positive runt pulse into a useable pulse or ignore it if it is too small. Normal propagation delays from the clock to Q may be extended in this configuration but the outputs will not be corrupted in any manner. Figure 2 does the same for a negative pulse. (Note: The 74F50729 can be used in a similar manner, but with the feedback originating from the opposite output.)

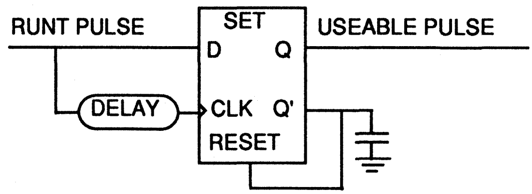


FIGURE 1—Blocks Positive Glitches

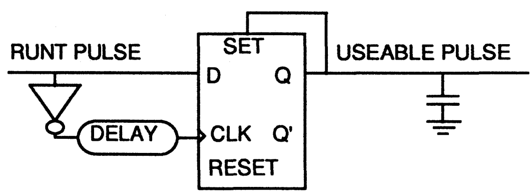


FIGURE 2—Blocks Negative Glitches

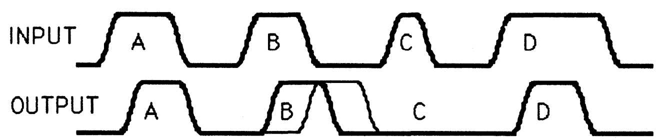


FIGURE 3 - Outputs of FIGURE 1 circuit compared to its input signal

The circuit is normally in the reset state (the Q output low) in Figure 1. If a glitch that is narrower than the delay (4 nanoseconds or wider works fine) arrives at the D input, the glitch on the data line will be gone when the clock sees the glitch and so the output will remain low. This is indicated in Figure 3 by the input C pulse not appearing on the output. If the glitch is the same size as the delay so that the data is in transition when the flip-flop clocks the outputs may switch with a delayed propagation time but they won't glitch (indicated by the B pulse in Figure 3). This is because the clock width is at least as long as the delay and is sufficient for the flip-flop to operate properly. If the input pulse is longer than the delay the output will have normal transitions (pulses A and D). The output of the device will be a pulse with a width determined by the characteristics of the output loading on Q'. With a 50 pf capacitor on the Q' output, the Q output pulse width is about 6ns. If a longer output pulse width is required, a non-inverting delay from the Q' to the reset or an inverting delay from the Q can be used. The width of the output pulse would then be about the propagation delay thru the flip-flop plus the delay to the reset input.

This circuit will only work with the metastable-immune features of the 74F50XXX series. If a non-metastable immune device is used the outputs can produce a glitch.

NOTES

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of seven series of handbooks:

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